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DIPARTIMENTO DI INGEGNERIA DELL'INFORMAZIONE

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Master Degree on Electronic Engineering

AICD report

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Contents

1 Laboratory activity n°1: Analysis and Design of CMOS Current Mirrors

1.1 DC and AC analysis of the basic current mirror

When V_1 increases from 0 to 1.2 V, I_{OUT} initially remains approximately constant with a slight positive slope due to channel-length modulation while M2 is in saturation. Once M2 enters triode, I_{OUT} drops steeply. The identity $I_{OUT} = N \cdot I_{IN}$ holds only at $V_1 = V_{GS,M1}$: at this specific point both M1 and M2 share the same $V_{DS} = V_{GS}$, so the channel-length modulation factor $(1 + \lambda V_{DS})$ is identical for both transistors and cancels in the ratio I_{OUT}/I_{IN}. For any other value of V_1, M2 has a different V_{DS} from M1, introducing a systematic error in the mirroring ratio.
Hand calculations for $W/L = 3.5\,\mu\text{m}/500\,\text{nm}$, $I_{REF} = 100\,\mu\text{A}$, using $\lambda = \lambda' \cdot L$:

$$\lambda = 1.1 \times 10^{7} \cdot 500 \times 10^{-9} = 5.5 \times 10^{-3}\,\text{V}^{-1} \tag{1}$$

$$g_m = \sqrt{2k'\frac{W}{L}I_D} \approx 811\,\mu\text{S} \tag{2}$$

$$R_o^{(\text{CM})} = \frac{1}{\lambda I_D} \approx 1.82\,\text{M}\Omega \tag{3}$$

The output resistance can also be estimated from the slope of the DC plot in saturation:

$$R_o^{(\text{DC})} = \left.\frac{\Delta V_1}{\Delta I_{OUT}}\right|_{\text{saturation}} \tag{4}$$

From the AC magnitude plot (Figure 2), the low-frequency output admittance gives:

$$R_o^{(\text{AC})} = \frac{1}{|Y_{out}(f \to 0)|} \approx 1.82\,\text{M}\Omega \tag{5}$$

which is consistent with the hand calculation, confirming the validity of the small-signal model.

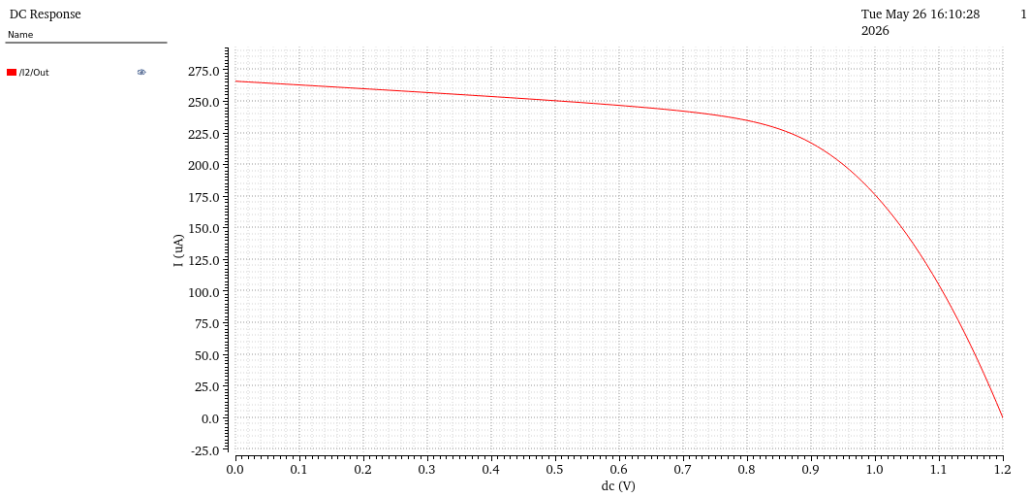


Figure 1: DC analysis of the basic current mirror: I_{OUT} vs V_1, with marker at $I_{OUT} = N \cdot I_{IN}$.

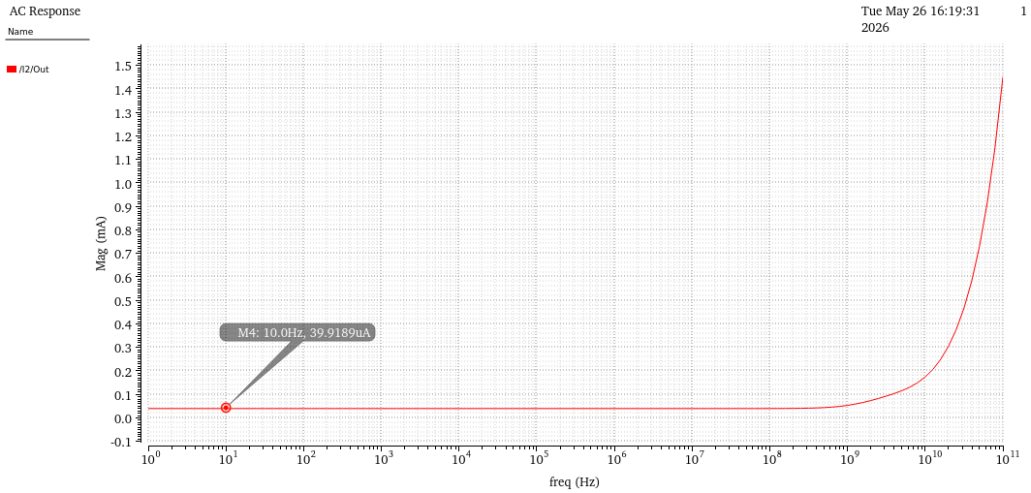


Figure 2: AC analysis of the basic current mirror: output admittance magnitude (dB).

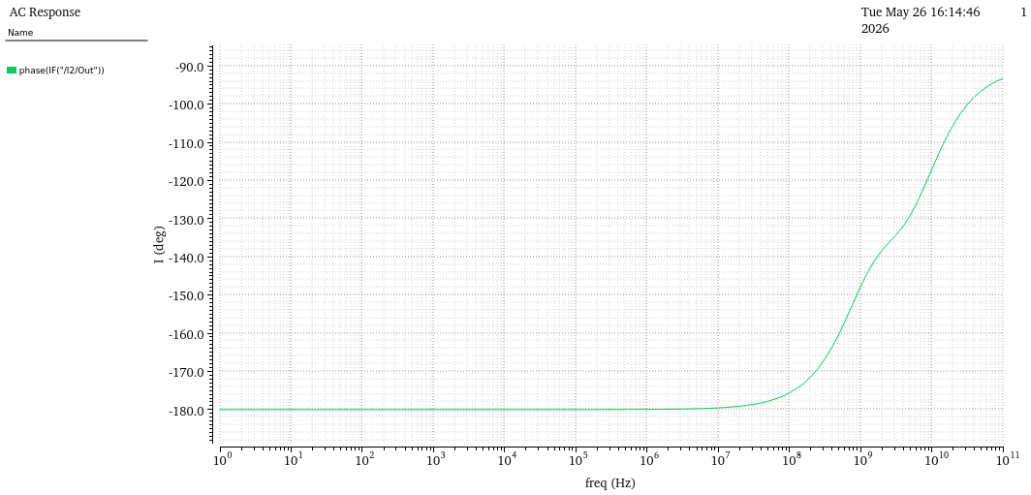


Figure 3: AC analysis of the basic current mirror: output admittance phase (°).

The phase goes from $-180°$ at low frequency to $-90°$ at high frequency, consistent with the output capacitance dominating Y_{out} at high frequency.
With $L_2 < L_1$, DIBL lowers V_{T2}, so M2 carries more current and $I_{OUT} > N \cdot I_{IN}$.
With narrower fingers on M2, the narrow-width effect raises V_{T2} (for $W \lesssim 1\,\mu$m), so M2 carries less current and $I_{OUT} < N \cdot I_{IN}$.

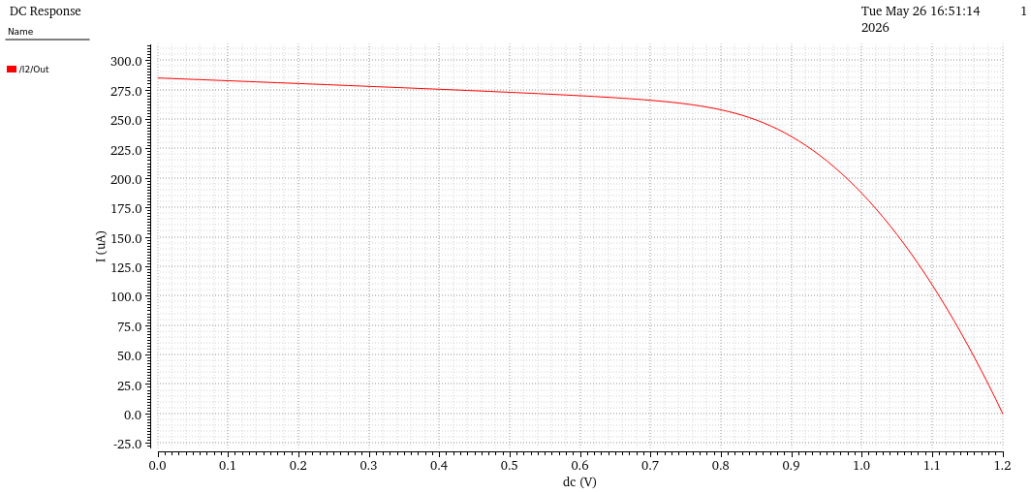


Figure 4: DC analysis of the basic current mirror: comparison of the three design variants (nominal, $L_1 \neq L_2$, different finger widths).

1.2 Process spread and device mismatch

Table 1: CM input voltage V_{IN} and output current error ΔI_O across process corners.

Parameter	**TYP (27°C)**	**SS (-20°C)**	**FF (85°C)**
V_{IN} (mV)	686	751.4	630.8
ΔI_O (μA)	-12.86	2.452	-23.46

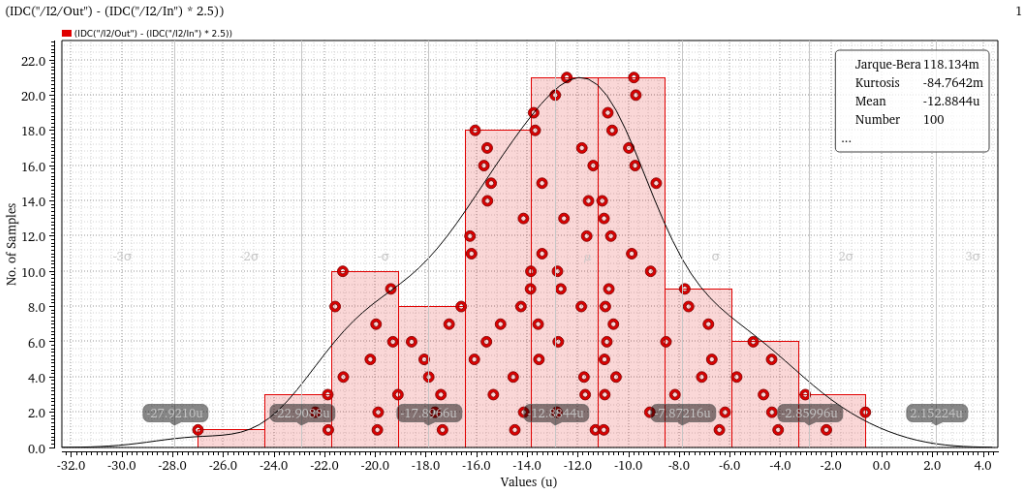
In the SS corner, k' is reduced and $|V_T|$ is higher, leading to a higher $V_{IN} = 751.4\,\text{mV}$; the FF corner shows the opposite trend with $V_{IN} = 630.8\,\text{mV}$. Regarding ΔI_O, in the SS corner the two transistors are shifted in the same direction by global process variation, resulting in a smaller error ($\Delta I_O = +2.452\,\mu\text{A}$), while in the FF corner the mismatch is more pronounced ($\Delta I_O = -23.46\,\mu\text{A}$).
The standard deviation of ΔI_O can be predicted by hand using the mismatch parameters $A_{\Delta V_T} = 5\,\text{mV} \cdot \mu\text{m}$ and $A_{\Delta k/k} = 1.1\,\% \cdot \mu\text{m}$. For $W = 3.5\,\mu\text{m}$, $L = 500\,\text{nm}$:

$$\sigma_{\Delta V_T} = \frac{A_{\Delta V_T}}{\sqrt{WL}} = \frac{5\,\text{mV} \cdot \mu\text{m}}{\sqrt{3.5 \cdot 0.5}\,\mu\text{m}} \approx 3.78\,\text{mV} \tag{6}$$

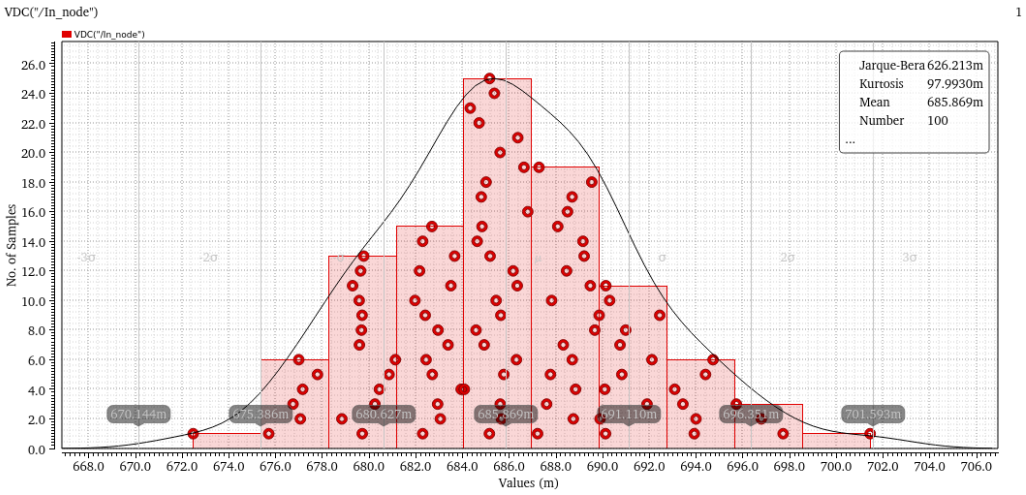
$$\sigma_{\Delta k/k} = \frac{A_{\Delta k/k}}{\sqrt{WL}} = \frac{1.1\,\% \cdot \mu\text{m}}{\sqrt{3.5 \cdot 0.5}\,\mu\text{m}} \approx 0.831\,\% \tag{7}$$

$$\frac{\sigma_{\Delta I_O}}{I_O} = \sqrt{\left(\sigma_{\Delta k/k}\right)^2 + \left(\frac{g_m}{I_D}\,\sigma_{\Delta V_T}\right)^2} = \sqrt{(0.831\,\%)^2 + (3.07\,\%)^2} \approx 3.18\,\% \tag{8}$$

which gives $\sigma_{\Delta I_O} = 3.18\,\% \times 250\,\mu\text{A} \approx 7.95\,\mu\text{A}$, reasonably consistent with the Monte Carlo result $= 5.01\,\mu\text{A}$, considering the approximations of the hand calculation model.



(a) Histogram of $\Delta I_O = I_{OUT} - 2.5 \cdot I_{IN}$: mean $= -12.88\,\mu$A, $\sigma = 5.012\,\mu$A.



(b) Histogram of V_{IN}: mean $= 685.9\,$mV, $\sigma = 5.241\,$mV.

Figure 5: Monte Carlo analysis (100 runs): histograms of ΔI_O and V_{IN} including both process spread and device mismatch.

The mean of ΔI_O is non-zero ($-12.88\,\mu$A) because global process variation shifts both transistors in the same direction, introducing a systematic offset in the mirroring ratio. Device mismatch, being a local variation, contributes only to the spread (σ) and not to the mean.
Regarding V_{IN}, the standard deviation from Monte Carlo ($\sigma = 5.24\,$mV) is significantly smaller than the range predicted by corner simulations ($V_{IN} \in [630.8,\ 751.4]\,$mV, range $= 120.6\,$mV), because corners represent worst-case extremes ($\pm 3\sigma$ or beyond) of the global process distribution, while Monte Carlo samples the full statistical distribution including both typical and extreme cases.

1.3 Wide-swing cascode current mirror

The n-type wide-swing cascode current mirror (WS-CCM) was sized as per the lab instructions. The width of the bias transistor M_6 was reduced to $W_6 = 1.1\,\mu$m ($L = 0.24\,\mu$m), iterating the dc operating point, so as to raise the cascode bias node until V_{DS}

of M_1–M_4 was $\approx 0.25\,\mathrm{V}$, i.e. all output-branch devices at the edge of saturation with equal headroom (Table 2).

Table 2: Key bias voltages of the WS-CCM at the dc operating point.

Quantity	Simulated value
$V_{DS,M1}$ [V]	0.227
$V_{DS,M2}$ [V]	0.230
$V_{DS,M3}$ [V]	0.222
$V_{DS,M4}$ [V]	0.270
$V_{G,M6}$ [V]	0.676

DC sweep and output current error

A dc sweep of the output voltage gives the I_{OUT}–V_{OUT} characteristic of Figure 6 (top). Reading the marker at $V_{OUT} - V_{IN} = 0.4\,\mathrm{V}$ ($V_{OUT} = 0.849\,\mathrm{V}$, $V_{IN} = 0.449\,\mathrm{V}$), with $N = 5$ and $I_{REF} = 100\,\mu\mathrm{A}$:

$$\varepsilon = |I_{OUT} - N\,I_{REF}| = |503.9 - 500| = 3.9\,\mu\mathrm{A}\ (= 0.78\,\%). \tag{9}$$

Output resistance

The output resistance is extracted from the low-frequency value of the ac output admittance magnitude (Figure 6, bottom):

$$R_o = \frac{1}{|Y_{out}|_{f\to 0}} = \frac{1}{7.41\,\mu\mathrm{S}} = 135\,\mathrm{k}\Omega. \tag{10}$$

The low-frequency phase of Y_{out} is flat, confirming its resistive nature, and rotates towards 90° only at high frequency, where the output capacitance dominates.

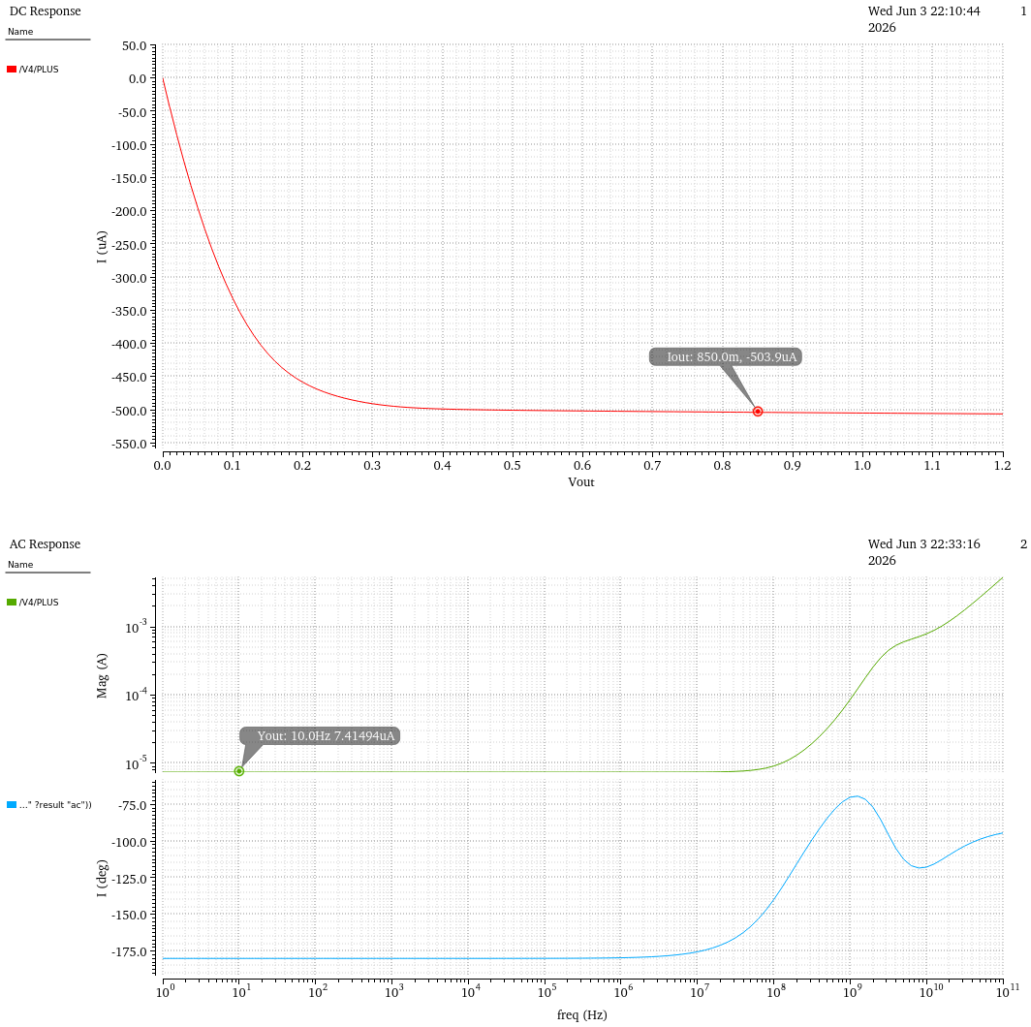


Figure 6: WS-CCM analysis. Top: I_{OUT} vs V_{OUT}; marker at $V_{OUT} = 0.849\,\mathrm{V}$ ($V_{OUT} - V_{IN} = 0.4\,\mathrm{V}$) reads $|I_{OUT}| = 503.9\,\mu\mathrm{A}$ ($\varepsilon = 0.78\,\%$). Bottom: magnitude and phase of Y_{out}; the 10 Hz marker gives $|Y_{out}| = 7.41\,\mu\mathrm{S}$, i.e. $R_o = 135\,\mathrm{k}\Omega$.

2 Laboratory activity n°2: Compensation of a Fully-Differential Two-Stage OTA with Capacitive Feedback

This laboratory session concerns the frequency-domain characterisation and Miller compensation of a fully-differential, two-stage OTA. The circuit topology adopts a p-type differential pair (M1–M2), an n-type current mirror load (M3–M6), a second gain stage formed by M7–M8 loaded by M9–M10, and a tail current source M12 biased by $I_{REF} = 50\,\mu\text{A}$. The design is required to satisfy the specifications listed in Table 3, derived from the overall capacitive-feedback amplifier requirements.

Table 3: OTA specifications for LAB02.

Specification	Value
Supply voltage V_{DD}	$1.2\,\text{V}$
Reference current I_{REF}	$50\,\mu\text{A}$
External load capacitance C_L	$1\,\text{pF}$
Low-frequency differential gain A_{dd0}	$\geq 30\,\text{dB}$
Gain-bandwidth product GBW	$\geq 1\,\text{GHz}$
Output voltage swing	$0.3\,\text{V} \leq V_{O1,2} \leq V_{DD} - 0.3\,\text{V}$
Offset voltage V_{OS}	$\leq 4\,\text{mV}$

The testbench (`tb_mirror_ota`) includes an ideal CMFB circuit with two $100\,\text{k}\Omega$ resistors, a VCVS with gain 1000, and a dc source setting the target output common-mode voltage; two $1\,\text{pF}$ load capacitors are placed at each output. An `ideal_balun` element generates the differential and common-mode input signals (V_{ID}, $V_{IC} = 0.4\,\text{V}$). The initial transistor sizing is reported in Table 4.

Table 4: Initial transistor sizing of the fully-differential current-mirror OTA.

Device	L [nm]	W_f [μm]	n_f	W [μm]
M1, M2	120	1.9	4	7.6
M3, M4	240	2.2	2	4.4
M5, M6	240	2.2	10	22.0
M7, M8	240	2.0	50	100.0
M9	240	2.0	20	40.0
M10	240	2.0	4	8.0
M12	240	—	—	—

2.1 DC Operating Point

Table 5 reports the simulated DC operating point of the OTA. For each transistor in one differential half-circuit, the drain current I_D, the drain-to-source voltage V_{DS}, the transconductance g_m, and the output resistance r_o are listed.

Table 5: Simulated DC operating point of the `mirror_ota` (one differential half-circuit).

Device	I_D (μA)	V_{DS} (mV)	g_m (μS)	r_o (kΩ)
M1	-27.37	-489.37	251.748	41.5734
M2	-27.37	-489.37	251.748	41.5734
M3	27.40	402.91	402.102	90.5337
M4	27.40	402.91	402.102	90.5337
M5	51.16	1000.74	606.624	72.7002
M6	51.16	1000.74	606.624	72.7002
M7	-51.14	-199.26	494.657	22.6895
M8	-51.14	-199.26	494.637	22.6895
M9	-54.75	-307.71	323.940	36.6314
M10	-50.00	-582.82	291.941	89.3272

The OTA is verified to be balanced by checking that each pair of symmetric transistors (M1–M2, M3–M4, M5–M6, M7–M8) exhibits identical operating conditions. From Table 5, all symmetric pairs share the same I_D, V_{DS}, g_m, and r_o to within simulation numerical precision (the small discrepancy observed for M7 and M8, where g_m differs by $0.020\,\mu$S, is negligible). The OTA is therefore confirmed to be well balanced.

Figure 7 shows the differential output voltage $V_{OD} = V_{O1} - V_{O2}$ and the common-mode output voltage $V_{OC} = (V_{O1} + V_{O2})/2$ as a function of the differential input voltage V_{ID}. V_{OD} exhibits the expected S-shaped transfer characteristic, ranging from approximately $+0.4\,$V to $-0.4\,$V, while V_{OC} remains constant at $1\,$V, confirming that the ideal CMFB circuit is regulating the output common-mode voltage correctly.

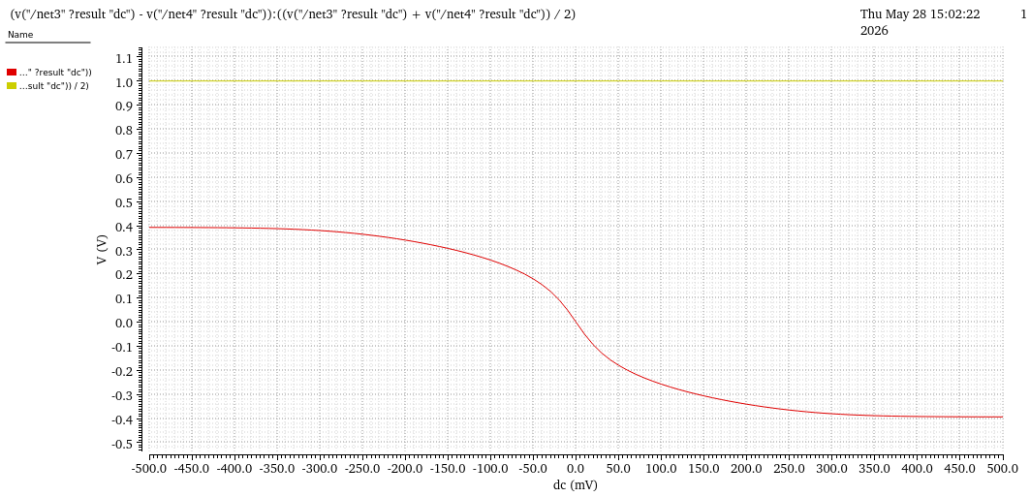


Figure 7: Differential output voltage V_{OD} (red) and common-mode output voltage V_{OC} (yellow) vs. differential input voltage V_{ID}.

Figure 8 shows the drain currents of the differential pair transistors M1 and M2 as a function of V_{ID}. The two curves are perfectly symmetric: at $V_{ID} = 0$, both currents equal approximately $-27.37\,\mu$A (half the tail current); as V_{ID} increases, the current steers entirely towards one transistor. The symmetry of the two curves further confirms that the OTA is well balanced.

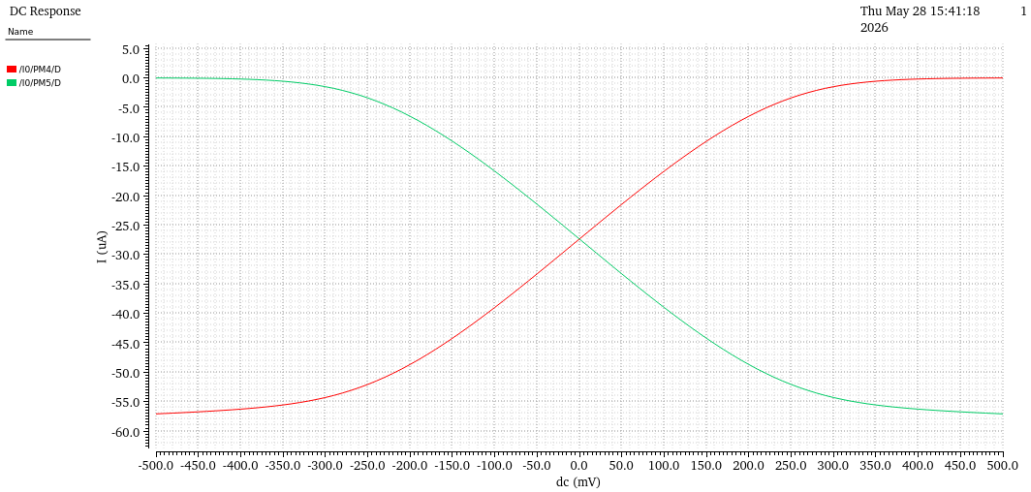


Figure 8: Drain currents of the differential pair transistors M1 (red) and M2 (green) vs. differential input voltage V_{ID}.

The simulation results match the expected behaviour. The S-shaped characteristic of V_{OD} confirms that the differential pair steers the tail current correctly between M1 and M2 as V_{ID} varies. The constant $V_{OC} \approx 1\,\mathrm{V}$ demonstrates that the ideal CMFB is effectively rejecting common-mode disturbances. The drain current curves of M1 and M2 are perfectly symmetric and cross at $V_{ID} = 0$, where each transistor carries half the tail current ($\approx 27.37\,\mu\mathrm{A}$), as expected for a balanced differential pair. No anomalies or asymmetries are observed.

2.2 Frequency response of the two-stage OTA (initial design, no compensation)

The uncompensated OTA is simulated with an AC sweep from 1 Hz to 100 GHz (logarithmic, 10 points per decade). Figure 9 shows the magnitude of the differential-mode voltage transfer function $A_{dd}(f)$, with markers placed at the low-frequency gain A_{dd0}, the $-3\,\mathrm{dB}$ bandwidth $f_{-3\mathrm{dB}}$, and the unity-gain frequency f_u. Figure 10 shows the corresponding phase response, with a marker at f_u indicating the phase margin PM. The simulated key parameters are summarised in Table 6.

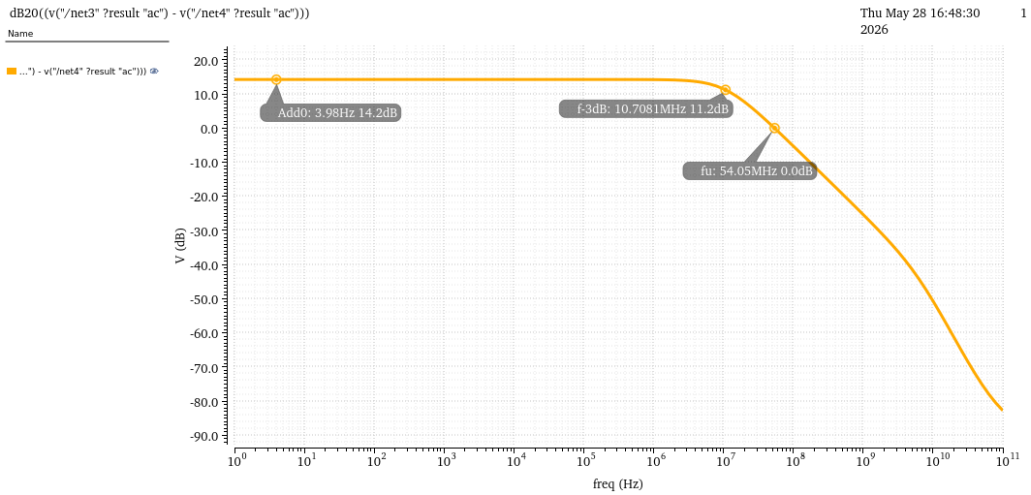


Figure 9: Magnitude of the differential-mode transfer function $A_{dd}(f)$ of the uncompensated OTA. Markers: $A_{dd0} = 14.2\,\text{dB}$, $f_{-3\text{dB}} = 10.708\,\text{MHz}$, $f_u = 54.05\,\text{MHz}$.

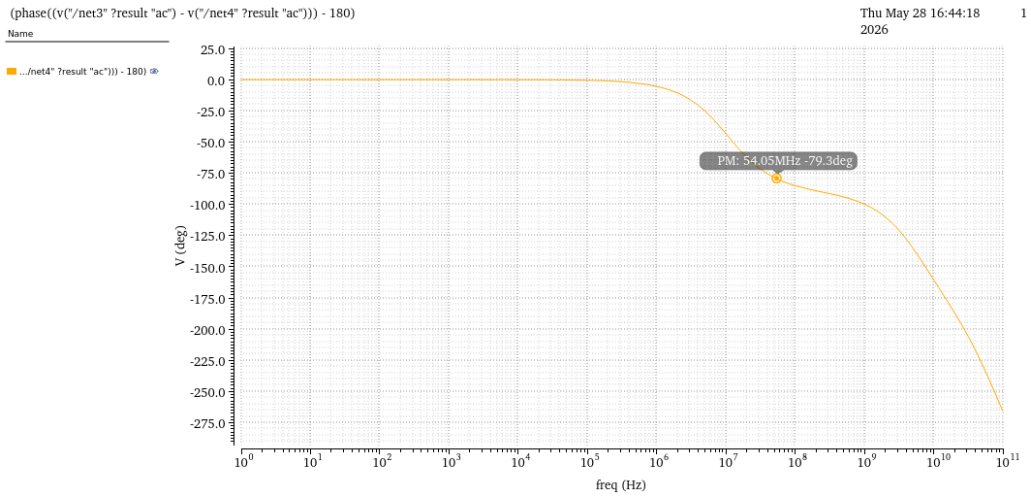


Figure 10: Phase of the differential-mode transfer function $A_{dd}(f)$ of the uncompensated OTA. Marker PM: phase $= -79.3°$ at $f_u = 54.05\,\text{MHz}$.

Table 6: Key parameters of the uncompensated OTA (simulated).

Parameter	Simulated	Specification
A_{dd0} [dB]	14.2	≥ 30
$f_{-3\text{dB}}$ [MHz]	10.708	—
f_u (GBW) [MHz]	54.05	≥ 1000
Phase margin [°]	-79.3	—

The simulated results show that the uncompensated OTA does not meet the specifications: $A_{dd0} = 14.2\,\text{dB}$ is well below the required 30 dB, and $f_u = 54.05\,\text{MHz}$ is far below the required 1 GHz GBW. As a consistency check, the GBW can be estimated as GBW $= A_{dd0,\text{lin}} \times f_{-3\text{dB}} = 5.13 \times 10.708\,\text{MHz} \approx 54.9\,\text{MHz}$, which closely matches f_u, confirming that the non-dominant pole f_{nd} is sufficiently larger than f_u. The phase margin of

$-79.3°$ is negative, confirming that the uncompensated OTA would be unstable in any closed-loop configuration. From the phase plot, the non-dominant pole can be estimated at $f_{nd} \approx 100$–$200\,\text{MHz}$, where the phase begins to drop steeply beyond the first-pole contribution.

2.3 Common-mode frequency response

To determine the common-mode gain, the AC component of V_{ID} is set to $0\,\text{V}$ and that of V_{IC} to $1\,\text{V}$, while the DC operating point is kept unchanged. Figure 11 shows the Bode plot of the common-mode transfer function $A_{cc}(f)$.

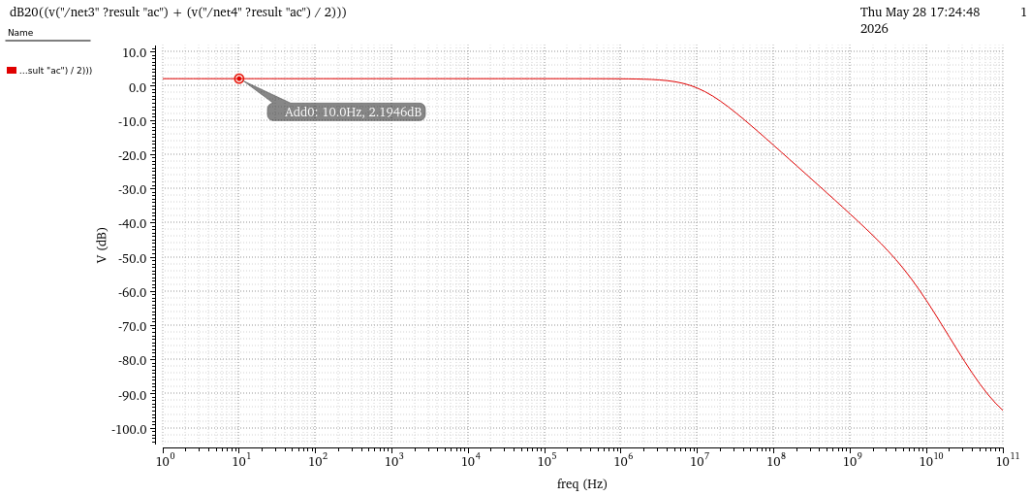


Figure 11: Common-mode transfer function $A_{cc}(f)$ of the uncompensated OTA. Marker: $A_{cc0} = 2.19\,\text{dB}$ at $10\,\text{Hz}$.

The low-frequency common-mode gain is $A_{cc0} = 2.19\,\text{dB}$, which is very low compared to the differential gain $A_{dd0} = 14.2\,\text{dB}$. The resulting CMRR is:

$$\text{CMRR} = A_{dd0} - A_{cc0} = 14.2 - 2.19 = 12.01\,\text{dB} \tag{11}$$

The very low common-mode gain is explained by the action of the ideal CMFB circuit: any common-mode perturbation at the output is sensed, amplified with gain 1000 by the ideal error amplifier, and fed back to the gate of the load transistors M7–M8, effectively suppressing the common-mode component. In a real circuit without ideal CMFB, the common-mode gain would be determined by the finite output impedance of the tail current source, and the CMRR would be much lower.

2.4 Offset Voltage and Design Adjustment

Offset definition

The offset voltage is the standard deviation of the mismatch-induced input voltage V_{MIS}, defined through the input–output relation of a fully-differential amplifier with mismatch, $V_{OD} = A_{dd0}(V_{ID} - V_{MIS})$, so that $V_{OS} = \sigma(V_{MIS})$. It is extracted from a 200-run Monte Carlo mismatch simulation in `tb_vos_mirror_ota`, where the OTA is closed in feedback through the two equal resistors R_2 (connected with opposite sign to avoid positive feedback). Each run settles with $V_{ID} = V_{MIS}$, so that $\sigma(V_{ID})$ directly measures V_{OS}.

Initial design

The Monte Carlo simulation on the initial sizing ($W_{1,2} = 7.6\,\mu\text{m}$, $L_{1,2} = 120\,\text{nm}$) gives the V_{ID} and V_{OD} distributions of Figures 12 and 13, from which

$$V_{OS} = \sigma(V_{ID}) = 4.918\,\text{mV} > 4\,\text{mV}. \tag{12}$$

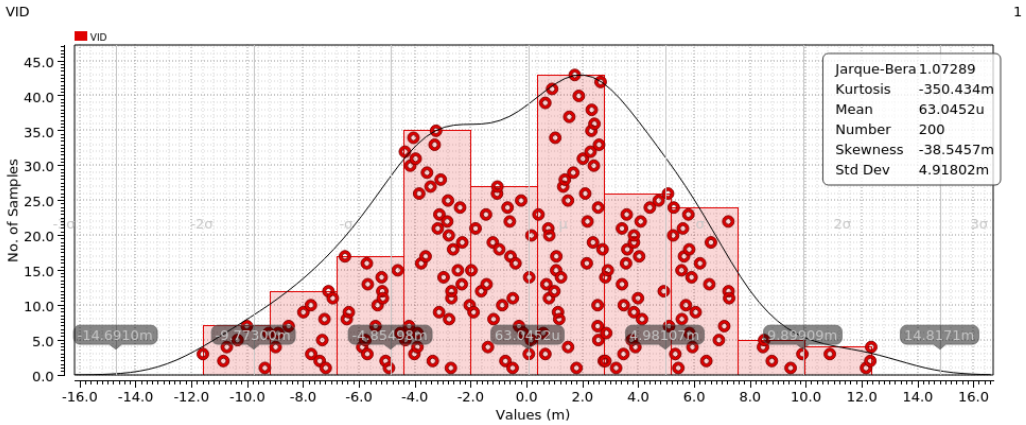


Figure 12: Monte Carlo distribution of V_{ID} — initial design ($n = 200$). Mean $= 63.0\,\mu\text{V}$, $\sigma = 4.918\,\text{mV}$.

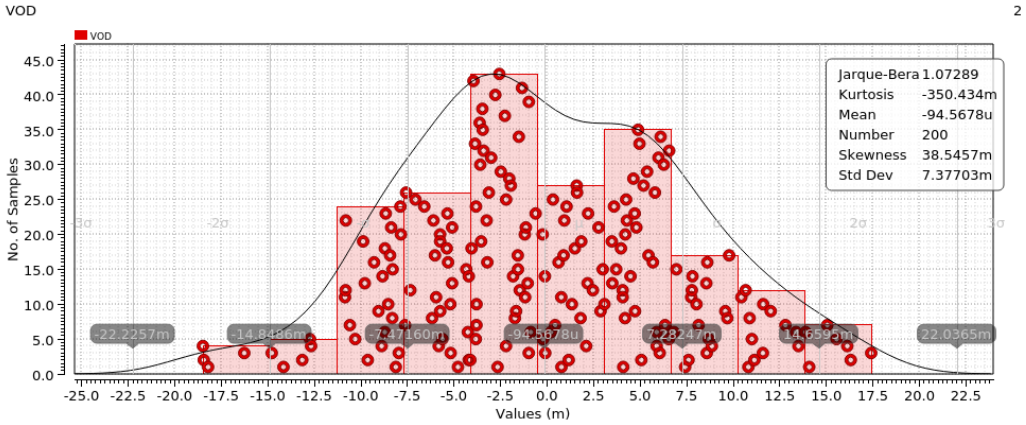


Figure 13: Monte Carlo distribution of V_{OD} — initial design ($n = 200$). Mean $= -94.6\,\mu\text{V}$, $\sigma = 7.377\,\text{mV}$.

The ratio $\sigma(V_{OD})/\sigma(V_{ID}) = 7.377/4.918 = 1.50$ is *not* equal to the open-loop gain ($A_{dd0,\text{lin}} = 5.13$, 14.2 dB): in the offset testbench the OTA works in closed loop, so both quantities follow the closed-loop transfer and the ratio is of order unity. Regardless of the loop gain, the feedback forces $V_{ID} = V_{MIS}$, hence $\sigma(V_{ID})$ yields V_{OS}. The offset is dominated by the threshold mismatch of the input pair:

$$\sigma_{V_{OS}}^{(M_1,M_2)} = \frac{A_{\Delta V_T,p}}{\sqrt{W_{1,2}L_{1,2}}} = \frac{3.6}{\sqrt{7.6\,\mu\text{m} \times 0.12\,\mu\text{m}}} = 3.77\,\text{mV}, \tag{13}$$

the remainder coming from the nMOS mirrors M_3–M_6. The AC analysis of the same design gives $A_{dd0} \approx 14.2\,\text{dB}$ and GBW $\ll 1\,\text{GHz}$: the initial design therefore fails all three specifications and is revised.

Design adjustment

The two specifications are governed by nearly independent quantities,

$$\mathrm{GBW} = \frac{G_M}{2\pi C_L}, \qquad A_{dd0} = G_M R_o, \qquad G_M = M\, g_{m1}, \quad R_o = r_{o5} \| r_{o7}, \tag{14}$$

where M is the mirror ratio ($\mathrm{M_3} \rightarrow \mathrm{M_5}$): G_M (and GBW) is fixed by the bias current, while R_o (the gain at given GBW) is fixed by the output-device length. The GBW specification sets $G_M \geq 2\pi C_L\,\mathrm{GBW} = 6.28\,\mathrm{mS}$. The design is then obtained with the following choices:

- $M = 7.5$ and tail multiplier $N = W_9/W_{10} = 6$, giving $I_{D1} = N I_{REF}/2 = 150\,\mu\mathrm{A}$ and a simulated $g_{m1} = 2.51\,\mathrm{mS}$ ($G_M \approx 18.8\,\mathrm{mS}$). N is raised above the LCM value to compensate the output-node parasitic loading discussed below; the output-branch current is $I_{D5} = I_{D7} = M I_{D1} \approx 1.11\,\mathrm{mA}$.
- $L_7 = L_8 = 1\,\mu\mathrm{m}$ to raise r_{o7} and meet $A_{dd0} \geq 30\,\mathrm{dB}$.
- $L_3 = L_5 = 500\,\mathrm{nm}$ (short) to keep the current-mirror-node pole above the unity-gain frequency.
- output common-mode $V_{OC} = 0.6\,\mathrm{V}$ (mid-rail), keeping the output transistors in saturation with symmetric swing within the 0.3 V to 0.9 V range.

The resulting sizing is given in Table 7 ($M = W_5/W_3 = 66/8.8 = 7.5$, $N = W_9/W_{10} = 48/8 = 6$). The larger input devices reduce the offset to

$$\sigma_{V_{OS}}^{(M_1,M_2)} = \frac{3.6}{\sqrt{44\,\mu\mathrm{m} \times 0.12\,\mu\mathrm{m}}} = 1.57\,\mathrm{mV} \leq 4\,\mathrm{mV}, \tag{15}$$

confirmed by a Monte Carlo run on the final sizing.

Table 7: Final transistor sizing ($M = 7.5$, $N = 6$, $V_{OC} = 0.6\,\mathrm{V}$).

Device	L [nm]	W_f [µm]	n_f	W [µm]
$\mathrm{M_1}$, $\mathrm{M_2}$	120	2.2	20	44.0
$\mathrm{M_3}$, $\mathrm{M_4}$	500	2.2	4	8.8
$\mathrm{M_5}$, $\mathrm{M_6}$	500	2.2	30	66.0
$\mathrm{M_7}$, $\mathrm{M_8}$	1000	4.0	90	360.0
$\mathrm{M_9}$	240	2.0	24	48.0
$\mathrm{M_{10}}$	240	2.0	4	8.0

Final results

The DC operating point of one balanced half-circuit is reported in Table 8; all devices are in saturation. The output resistance $R_o = r_{o5} \| r_{o7} = 4.38\,\mathrm{k\Omega} \| 20.05\,\mathrm{k\Omega} \approx 3.6\,\mathrm{k\Omega}$ together with $G_M = M\, g_{m1} \approx 18.8\,\mathrm{mS}$ gives $A_{dd0} \approx 36.6\,\mathrm{dB}$, in close agreement with the 35.1 dB measured in the AC response of Figure 14.

The DC currents and the balanced operating point match the design. The simulated r_o values are lower than the LCM prediction because of short-channel effects, which is why the output length had to be increased to reach the gain target. The measured GBW = 1.06 GHz is below the ideal $G_M/(2\pi C_L) \approx 3\,\mathrm{GHz}$ because the wide output devices add parasitic capacitance to the output node ($C_{out} \approx 2.8\,\mathrm{pF}$, i.e. $\sim 1.8\,\mathrm{pF}$ on top of C_L); this is compensated by the bias-current margin. All specifications are met (Table 9).

Table 8: Simulated DC operating point (one differential half-circuit).

Device	I_D	V_{DS} [mV]	g_m [mS]	r_o [kΩ]
M_1 (p)	148.6 µA	−256	2.51	4.13
M_3 (n)	148.6 µA	+503	1.35	30.39
M_5 (n)	1.11 mA	+600	10.25	4.38
M_7 (p)	1.11 mA	−600	7.59	20.05

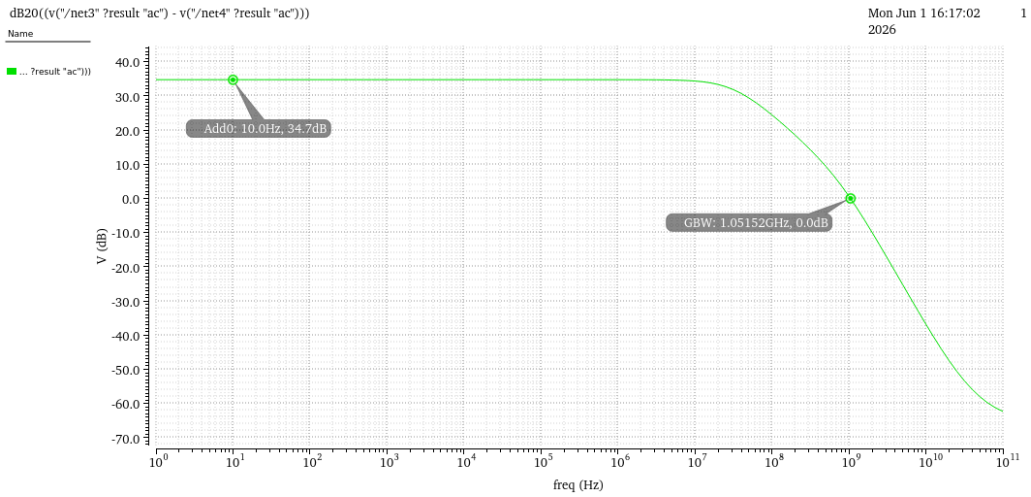


Figure 14: Differential AC response of the final design: $A_{dd0} = 35.1\,\text{dB}$ and GBW = 1.06 GHz.

Table 9: Performance summary of the final OTA design.

Parameter	Simulated	Specification	Status
A_{dd0} [dB]	35.1	≥ 30	✓
GBW [GHz]	1.06	≥ 1	✓
V_{OS} [mV]	1.57	≤ 4	✓

3 Design of a capacitive feedback amplifier based on a two-stage OTA

The circuit under study is an inverting amplifier built around a fully-differential, two-stage operational transconductance amplifier (OTA) closed in a capacitive feedback loop. In this configuration the low-frequency closed-loop gain is fixed by the ratio of the source and feedback capacitors,

$$A_\infty = -\frac{C_s}{C_f}, \tag{16}$$

and is therefore essentially insensitive to the large but poorly controlled open-loop gain of the OTA, as long as the loop gain is high enough. How accurately the ideal gain is approached is set by the loop gain $T_0 = \beta\, A_{dd0}$, where A_{dd0} is the differential DC gain of the OTA and β is the feedback factor of the capacitive divider seen at the inverting input. The static and dynamic (settling) errors are tied to the loop parameters by

$$\epsilon_0 \simeq \frac{1}{T_0}, \qquad \epsilon_d \simeq e^{-\omega_c t_s}, \tag{17}$$

so a large T_0 is required for a small ϵ_0 and a large crossover frequency ω_c for fast, accurate settling.

A two-stage OTA exposes two high-impedance internal nodes and hence two poles at comparable frequencies. Left uncompensated, the phase margin is small, the loop is strongly under-damped and the step response rings; in addition, the direct two-stage topology introduces a right-half-plane (RHP) zero that further erodes the phase margin. A Miller compensation network (a capacitor C_c between the two stages, in series with a nulling resistor R_z) is therefore added to split the poles and to relocate the RHP zero. The starting point is the uncompensated sizing of the lab instructions; the OTA is then redesigned to meet the target specifications.

3.1 Initial (uncompensated) design

3.1.1 DC operating point

The starting sizing uses a common channel length $L = 240\,\text{nm}$ for all devices, with the bias chain set by the reference current $I_{REF} = 50\,\mu\text{A}$. The annotated operating point, summarised in Table 10, confirms that every transistor is biased in saturation with a sensible overdrive.

Transistor	Width (W)	Length (L)	Current (I_d)	Overdrive (V_{ov})
M1	4.00 µm	240.0 nm	100.19 µA	139.9 mV
M2	4.00 µm	240.0 nm	100.19 µA	139.9 mV
M3	12.00 µm	240.0 nm	−100.15 µA	207.3 mV
M4	12.00 µm	240.0 nm	−100.15 µA	207.3 mV
M5	48.00 µm	240.0 nm	−444.19 µA	215.7 mV
M6	48.00 µm	240.0 nm	−444.19 µA	215.7 mV
M7	19.20 µm	240.0 nm	444.19 µA	129.8 mV
M8	19.20 µm	240.0 nm	444.18 µA	129.8 mV
M9A	4.80 µm	240.0 nm	101.46 µA	129.4 mV
M9B	4.80 µm	240.0 nm	98.84 µA	127.1 mV
M10	6.00 µm	240.0 nm	−50.00 µA	207.3 mV
M11	6.00 µm	240.0 nm	−53.56 µA	210.8 mV
M12	2.40 µm	240.0 nm	53.56 µA	129.6 mV

Table 10: DC operating point of the initial (uncompensated) design.

3.1.2 Open-loop frequency response

Starting from the operating point of Table 10, the differential DC gain and the dominant output pole estimated by hand are

$$A_{dd0} = g_{m1}\,(r_{o1} \parallel r_{o3}) \cdot g_{m5}\,(r_{o5} \parallel r_{o7}) = 52.66\,\text{dB}, \tag{18}$$

$$f_p = \frac{1}{2\pi\, C_L\, R_o} = 9.81\,\text{MHz}. \tag{19}$$

The corresponding AC simulation (Figure 15) returns $A_{dd0} = 46.98\,\text{dB}$ and a first pole at $f_{p1} = 7.94\,\text{MHz}$. The simulated gain sits a few dB below the analytical estimate because the long-channel model overestimates the device output resistances at these channel lengths: short-channel effects lower r_o, so the hand calculation should be read as an upper bound that must be verified in simulation.

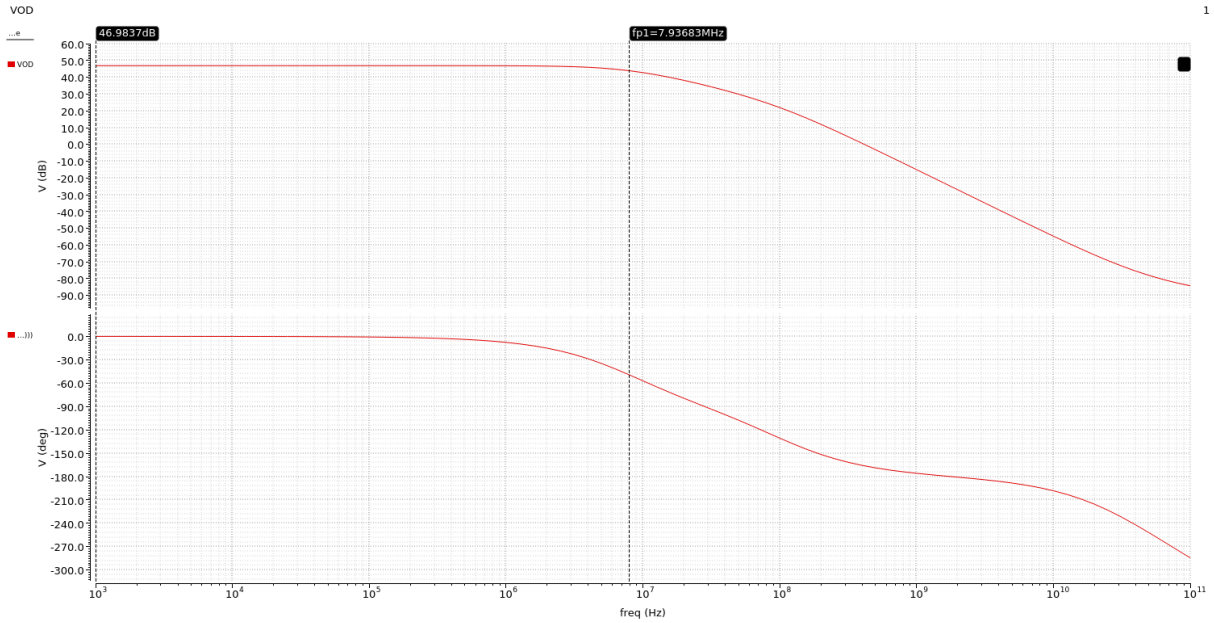


Figure 15: Open-loop differential frequency response of the initial design.

3.1.3 Loop transfer function

The loop gain is measured from the return differential signal $v_f(F_1) - v_f(F_2)$ obtained by breaking the loop at the OTA input. As shown in Figure 16, the DC loop gain is $T_0 = 37.4\,\text{dB}$ and the phase margin is only $PM \approx 25°$. The poor phase margin is the direct consequence of the two poles falling close together, compounded by the uncompensated RHP zero of the two-stage topology, and it anticipates the heavy ringing seen in the time-domain response.

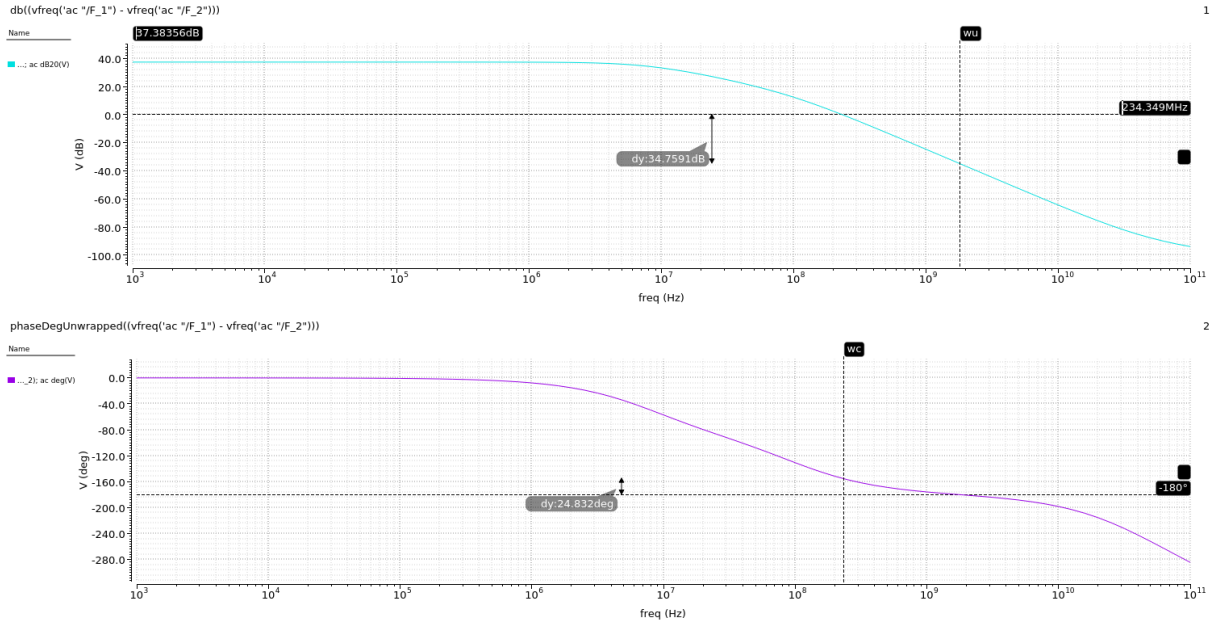


Figure 16: Loop transfer function of the initial design.

3.1.4 Transient response

In the open-loop test (Figure 17) the differential signal is not yet stabilised by feedback, so the large open-loop gain drives the differential output against the supply rails. Once the loop is closed (Figure 18), the step response exhibits a large overshoot followed by slowly-decaying ringing, fully consistent with the $\sim 25^\circ$ phase margin. The loop remains stable, in that the oscillation decays and the output eventually settles, but the response is far too under-damped and slow to meet the target settling time.

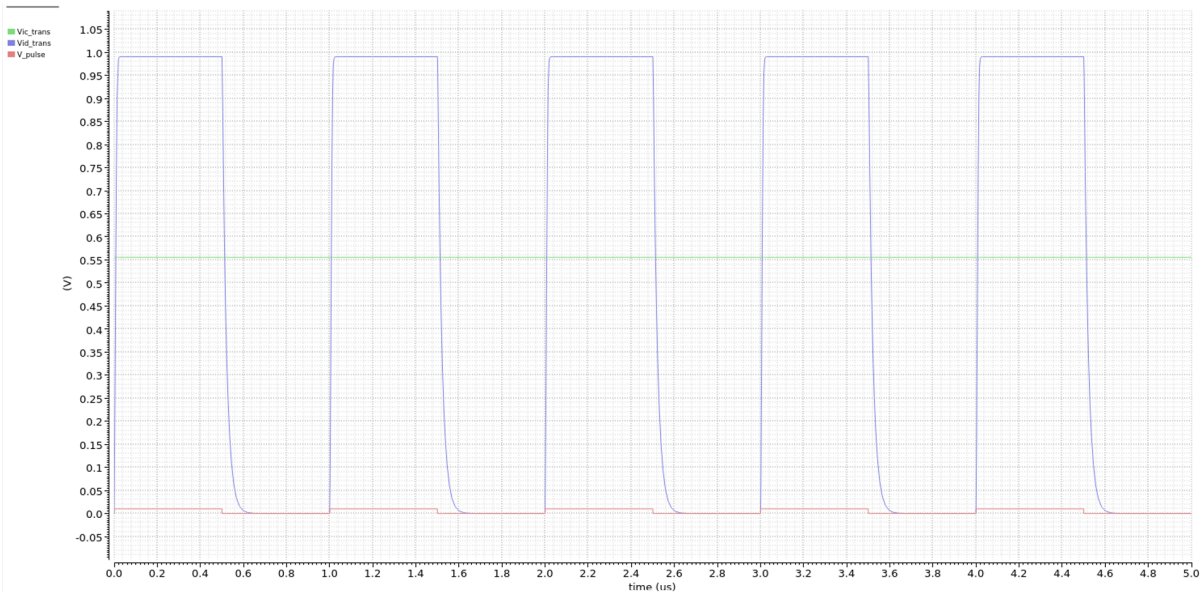


Figure 17: Open-loop step response of the initial design.

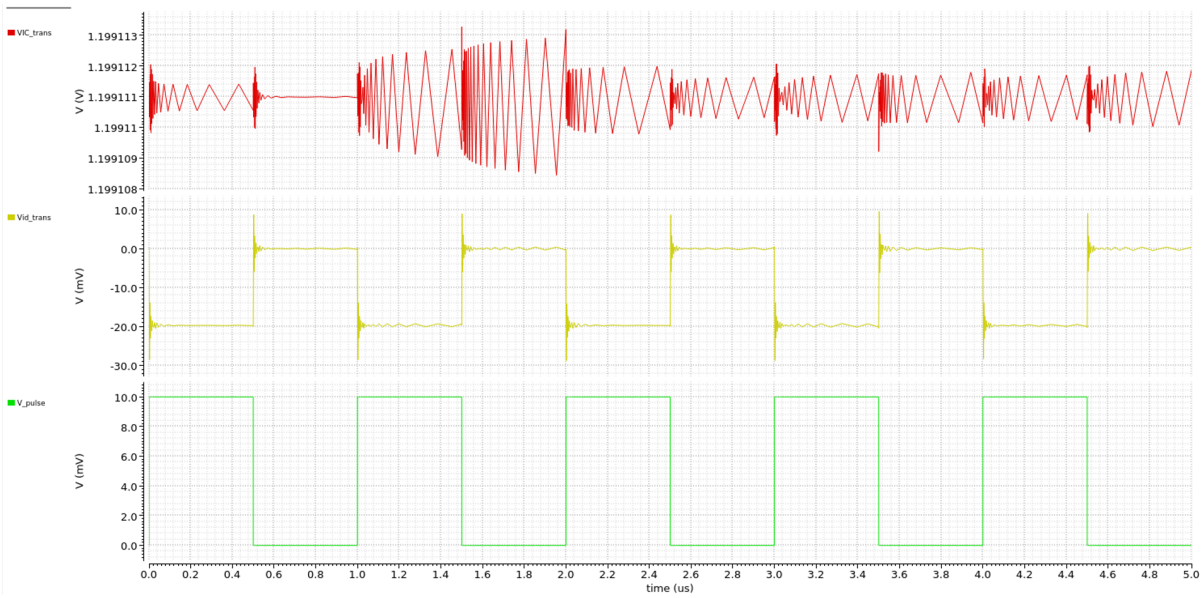


Figure 18: Closed-loop step response of the initial design.

3.1.5 Closed-loop frequency response

The closed-loop differential response (Figure 19) shows pronounced peaking (≈ 13 dB) around 200 MHz and a phase that swings down to -180°: this is the frequency-domain

signature of the low phase margin, and the RHP zero of the uncompensated two-stage topology is also visible. The DC closed-loop gain is $\approx 5.9\,\text{dB}$, i.e. a magnitude of about 2, in agreement with the ideal value $A_\infty = -2$.

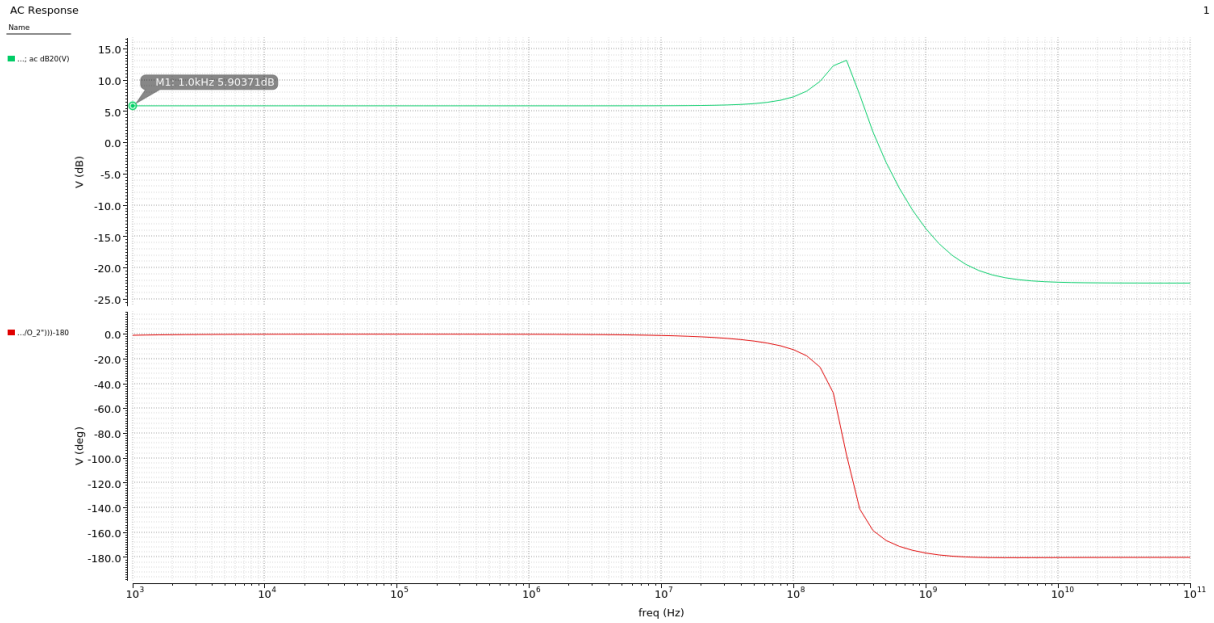


Figure 19: Closed-loop differential frequency response of the initial design.

3.2 Redesign for the target specifications

The OTA is redesigned to satisfy the following requirements:

1. Static error: $\epsilon_0 \leq 0.2\%$
2. Dynamic error: $\epsilon_d \leq 0.2\%$ at settling time $t_s = 20\,\text{ns}$
3. Phase margin: $PM \approx 70°$
4. Ideal closed-loop gain at low frequency: $A_\infty = -2$
5. OTA DC power consumption: $P_{DC} \leq 1.2\,\text{mW}$
6. Supply voltage: $V_{DD} = 1.2\,\text{V}$
7. OTA offset voltage: $V_{OS} \leq 2\,\text{mV}$
8. External load capacitance: $C_L = 4\,\text{pF}$
9. Source capacitance: $C_s = 1\,\text{pF}$
10. Reference current: $I_{REF} = 50\,\mu\text{A}$

3.2.1 Design procedure

1. Loop parameters. With $A_\infty = -2$ and an input parasitic capacitance $C_i = 10\,\text{fF}$, the feedback capacitor and the feedback factor follow from

$$C_f = -\frac{C_s}{A_\infty}, \qquad \beta = \frac{C_f}{C_s + C_f + C_i}. \tag{20}$$

The static-error and settling specifications then fix the required loop gain, the OTA DC gain and the crossover frequency:

$$T_0 = \frac{1-\epsilon_0}{\epsilon_0}, \qquad A_{dd0} = \frac{T_0}{\beta}, \qquad \omega_c = \frac{1}{t_s}\ln\!\left(\frac{1}{\epsilon_d}\right), \tag{21}$$

and the target gain-bandwidth product is $GBW = \omega_c/(2\pi\beta)$.

2. Small-signal parameters and biasing. The phase-margin specification sets the target transconductances G_{m1} and G_{m2}. With Miller compensation the dominant pole is pushed down to roughly $1/(G_{m2}R_1R_2C_c)$ while the second pole is moved up (pole splitting), and a feedforward RHP zero appears at $\omega_z = G_{m2}/C_c$. A compensation capacitor $C_c = 2\,\text{pF}$ was tried first, but simulations showed it was too large to reach the required ω_c; it was therefore reduced to $C_c = 1.5\,\text{pF}$. The ideal input transconductance is then

$$G_{m1,\text{ideal}} = \frac{\omega_c\, C_c}{\beta}, \tag{22}$$

and to keep enough margin against the non-dominant poles during settling the actual value was oversized by 50%, $G_{m1} = 1.5\, G_{m1,\text{ideal}}$.

The overdrives were chosen as $V_{ov1} = 0.1\,\text{V}$ and $V_{ov5} = 0.2\,\text{V}$ to keep all devices comfortably in saturation. The first- and second-stage bias currents are

$$I_{b1} = G_{m1}V_{ov1}, \qquad I_{b2} = \frac{G_{m2}V_{ov5}}{2}, \tag{23}$$

and the total power is verified against $P_{dc} = V_{dd}\,(2I_{b2} + I_{b1}) \le 1.2\,\text{mW}$. The per-stage equivalent resistances needed to reach the target gain are

$$R_2 = \sqrt{\frac{A_{dd0}}{G_{m1}G_{m2}}\frac{I_{b1}}{2I_{b2}}}, \qquad R_1 = \frac{A_{dd0}}{G_{m1}G_{m2}R_2}. \tag{24}$$

Finally, the nulling resistor relocates the RHP zero so that it no longer subtracts phase at the crossover (and, for $R_z > 1/G_{m2}$, can be turned into an LHP zero that partially cancels the second pole):

$$R_z = \frac{1+K}{G_{m2}}, \qquad K = \frac{G_{m2}}{\beta\, G_{m1}}\tan(\phi_z). \tag{25}$$

3. Transistor sizing. The channel lengths of the amplifying devices were fixed to $L_1 = 480\,\text{nm}$ and $L_5 = 360\,\text{nm}$. Using the stage resistances R_1 and R_2, the lengths of the load transistors follow from the required output resistances,

$$L_3 = \frac{r_{o3}\, I_{b1}}{2\,\mu_p}, \qquad L_7 = \frac{r_{o7}\, I_{b2}}{\mu_n}, \tag{26}$$

and the widths are then extracted from the square-law expression

$$W_i = \frac{L_i \, I_{d,i}}{k \, V_{ov,i}^2}. \tag{27}$$

The biasing devices reuse the layout of their references: M10 and M11 mirror the PMOS loads and share length and overdrive with M3, while M9 and M12 share the properties of M7.

4. Statistical offset. The input-referred offset is dominated by the first stage and is estimated from device mismatch as

$$V_{OS} = \sqrt{\left(\frac{V_{ov1}}{2}\right)^2 \left(\sigma_{k,n}^2 + \sigma_{k,p}^2\right) + \sigma_{Vn}^2 + \left(\frac{V_{ov1}}{V_{ov3}}\right)^2 \sigma_{Vp}^2}, \tag{28}$$

where the current-factor and threshold standard deviations follow Pelgrom's law, $\sigma_k = A_k/\sqrt{WL}$ and $\sigma_V = A_{vt}/\sqrt{WL}$.

3.2.2 Final transistor sizing

The resulting operating point is reported in Table 11.

Transistor	Width (W)	Length (L)	Current (I_d)	Overdrive (V_{ov})
M1	21.56 µm	480.0 nm	105.87 µA	75.4 mV
M2	21.56 µm	480.0 nm	105.87 µA	75.4 mV
M3	14.48 µm	620.0 nm	−105.77 µA	330.7 mV
M4	14.48 µm	620.0 nm	−105.77 µA	330.7 mV
M5	30.00 µm	360.0 nm	−374.64 µA	329.0 mV
M6	30.00 µm	360.0 nm	−374.64 µA	329.0 mV
M7	14.32 µm	810.0 nm	374.64 µA	315.1 mV
M8	14.32 µm	810.0 nm	374.64 µA	315.1 mV
M9A	3.08 µm	810.0 nm	78.83 µA	316.2 mV
M9B	5.00 µm	810.0 nm	132.70 µA	320.1 mV
M10	6.86 µm	620.0 nm	−50.00 µA	330.7 mV
M11	6.86 µm	620.0 nm	−50.14 µA	330.7 mV
M12	1.91 µm	810.0 nm	50.14 µA	314.8 mV

Table 11: DC operating point of the final (compensated) design.

3.2.3 Expected versus simulated performance

The hand calculation predicts $A_{dd0} = 63.56\,\text{dB}$, $T_0 = 53.96\,\text{dB}$, $\omega_c = 3.107 \times 10^8\,\text{rad}\,\text{s}^{-1}$ and a dominant pole at $f_{p1} = 99.1\,\text{kHz}$, with a power consumption

$$P_{DC} = V_{DD}\,(I_{b1} + 2I_{b2}) = 1.153\,\text{mW}. \tag{29}$$

As anticipated by the lab instructions, simulation departs somewhat from the hand calculation, and in particular the target on A_{dd0} is not fully met. The open-loop response (Figure 20) gives

1. $A_{dd0} = 54.03\,\text{dB}$
2. $f_{p1} = 295.5\,\text{kHz}$

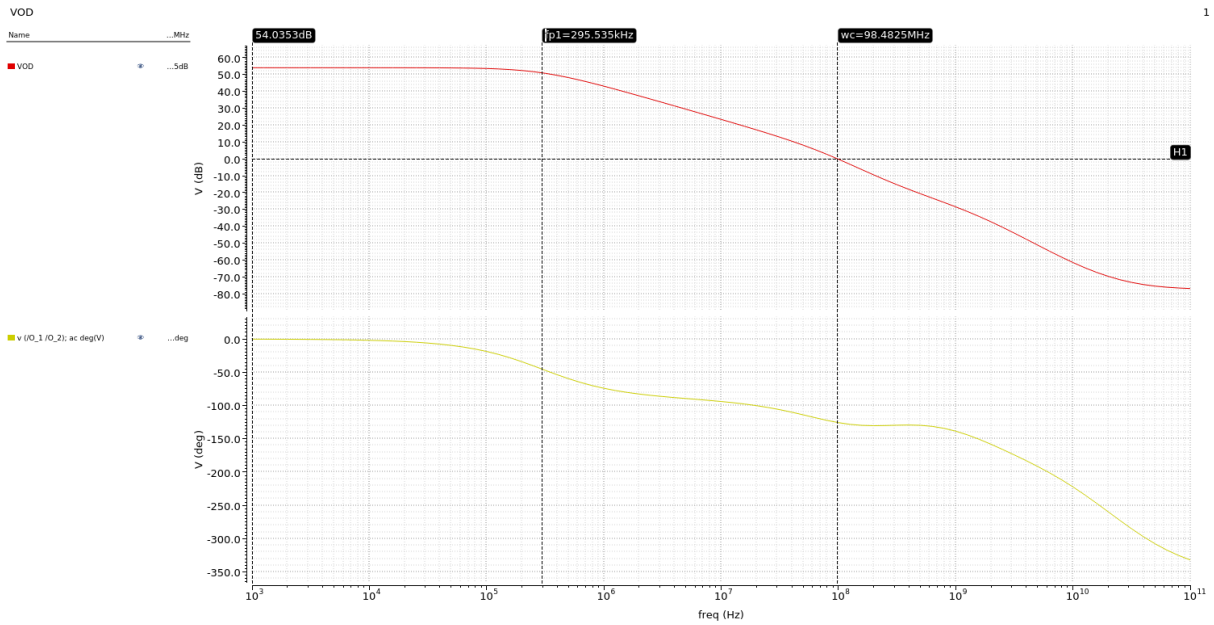


Figure 20: Open-loop differential frequency response of the final design.

From the loop transfer function (Figure 21) the loop gain, phase margin and crossover are

1. $T_0 = 44.44\,\text{dB}$
2. $PM = 68.5°$
3. $f_c = 43.82\,\text{MHz} \;\rightarrow\; \omega_c = 2.754 \times 10^8\,\text{rad}\,\text{s}^{-1}$

which yields a static error $\epsilon_0 = 0.6\%$. The residual gap with respect to the 0.2% target traces back to the lower-than-predicted output resistances in simulation: short-channel effects cap the achievable A_{dd0}, and hence T_0, below the long-channel estimate. Closing this gap would require longer output devices at the cost of bandwidth and area.

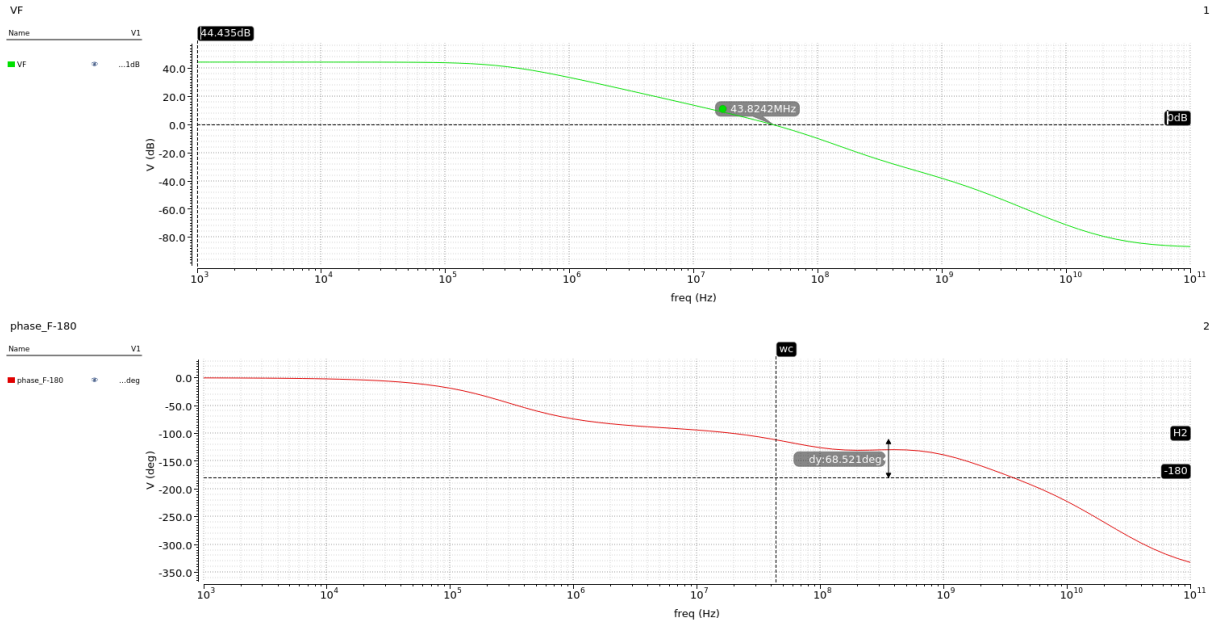


Figure 21: Loop transfer function of the final design.

3.2.4 Transient response

Thanks to the compensation network, the closed-loop step response settles cleanly and with a markedly smaller overshoot than the uncompensated design. From the zoom on the settling shown in Figure 22, with $v(t_s) = -19.917\,\text{mV}$ and $v(\infty) \approx -19.887\,\text{mV}$, the dynamic error is

$$\epsilon_d = \frac{|v(\infty) - v(t_s)|}{|v(\infty)|} = 0.15\%. \tag{30}$$

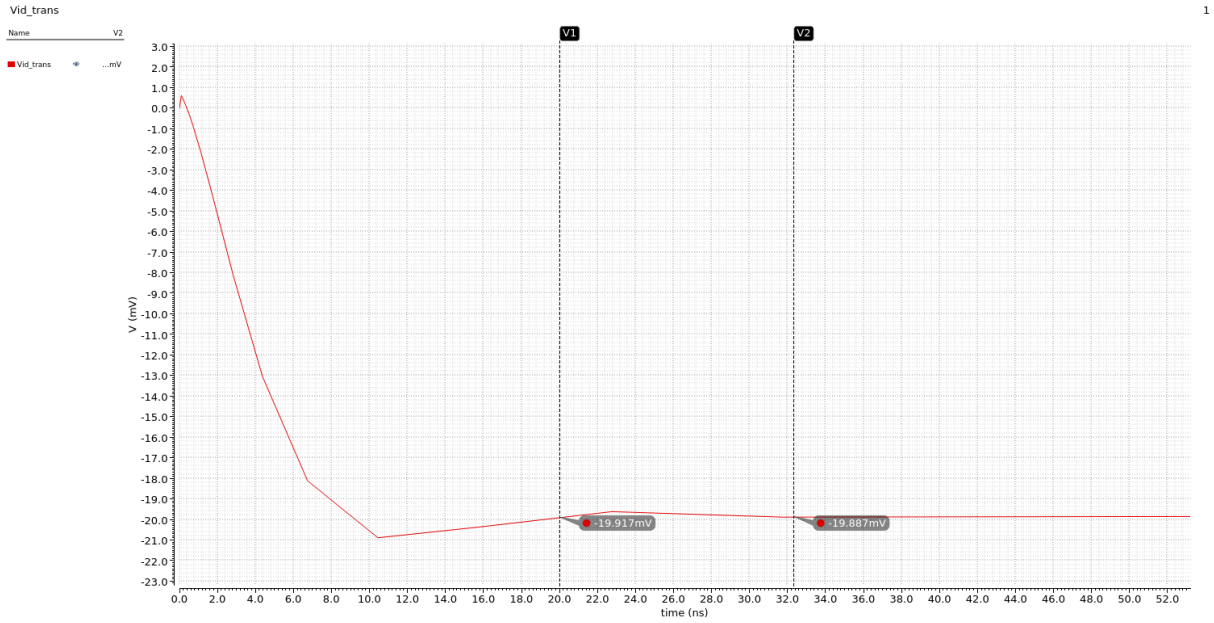


Figure 22: Closed-loop step response of the final design.

3.2.5 Closed-loop frequency response

The closed-loop differential response of Figure 23 is smooth and free of the peaking seen in the initial design, confirming the high phase margin; the RHP zero has been effectively compensated and the DC gain is $\approx 6\,\text{dB}$, i.e. $A_\infty = -2$.

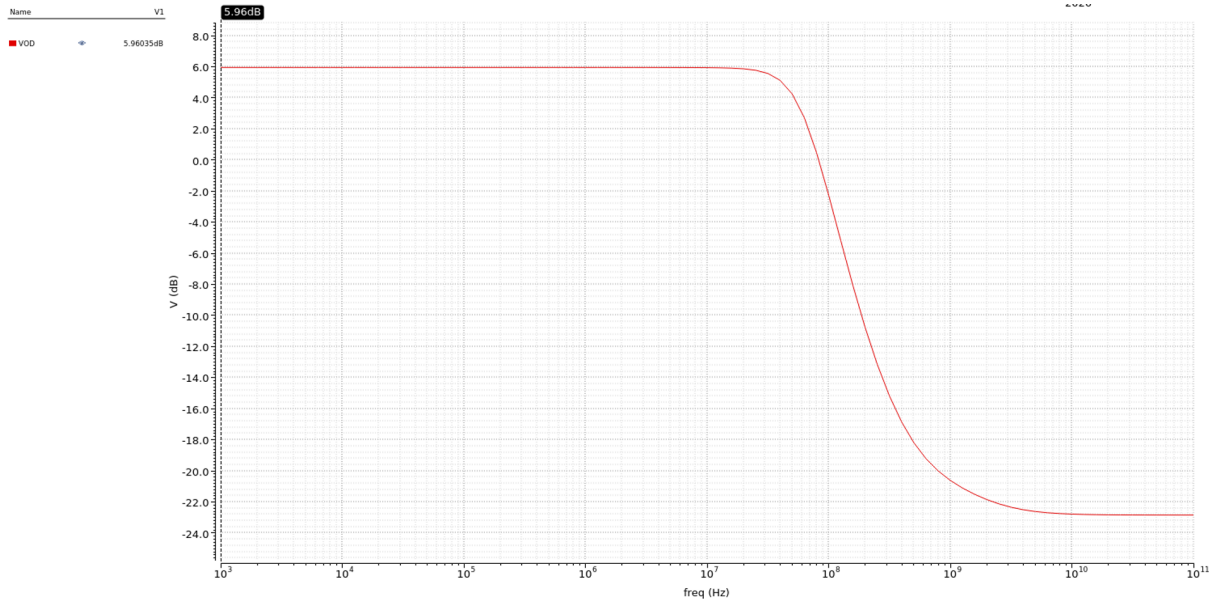


Figure 23: Closed-loop differential frequency response of the final design.

3.2.6 Offset voltage

The offset voltage is extracted as the standard deviation of the input differential voltage V_{ID} over a 100-run Monte Carlo simulation. From Figure 24 the distribution is approximately Gaussian and gives $V_{OS} = 1.612\,42\,\text{mV}$, comfortably below the 2 mV specification.

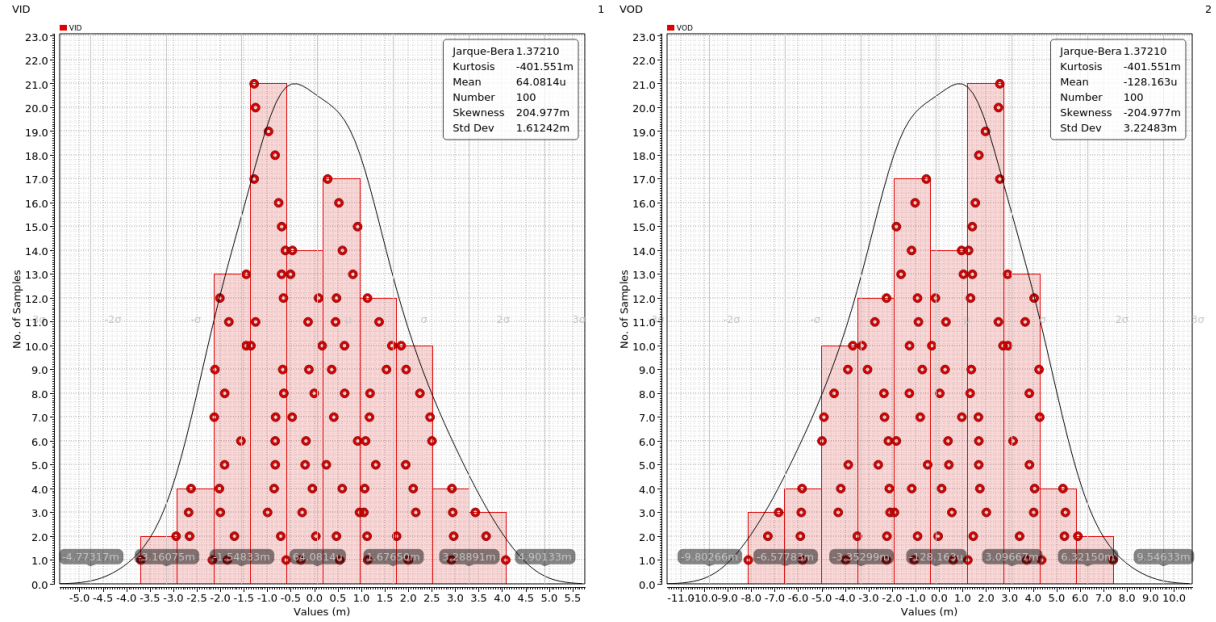


Figure 24: Monte Carlo estimation of the offset voltage V_{OS}.

3.2.7 Summary of results

All specifications are met except the static error, as summarised in Table 12.

Specification	**Target**	**Achieved**	**Status**
Static error ϵ_0	$\leq 0.2\%$	0.6%	$\times$
Dynamic error ϵ_d	$\leq 0.2\%$	0.15%	✓
Phase margin PM	$\approx 70°$	$68.5°$	✓
Closed-loop gain A_∞	-2	-2	✓
Power consumption P_{DC}	$\leq 1.2\,\text{mW}$	$1.153\,\text{mW}$	✓
Offset voltage V_{OS}	$\leq 2\,\text{mV}$	$1.61\,\text{mV}$	✓

Table 12: Summary of the target specifications and the simulated results of the final design.

4 Laboratory activity n°4: Design of a Low-Voltage Band-Gap Voltage Reference

4.1 Preliminary design of the LV-BGR

Circuit schematic

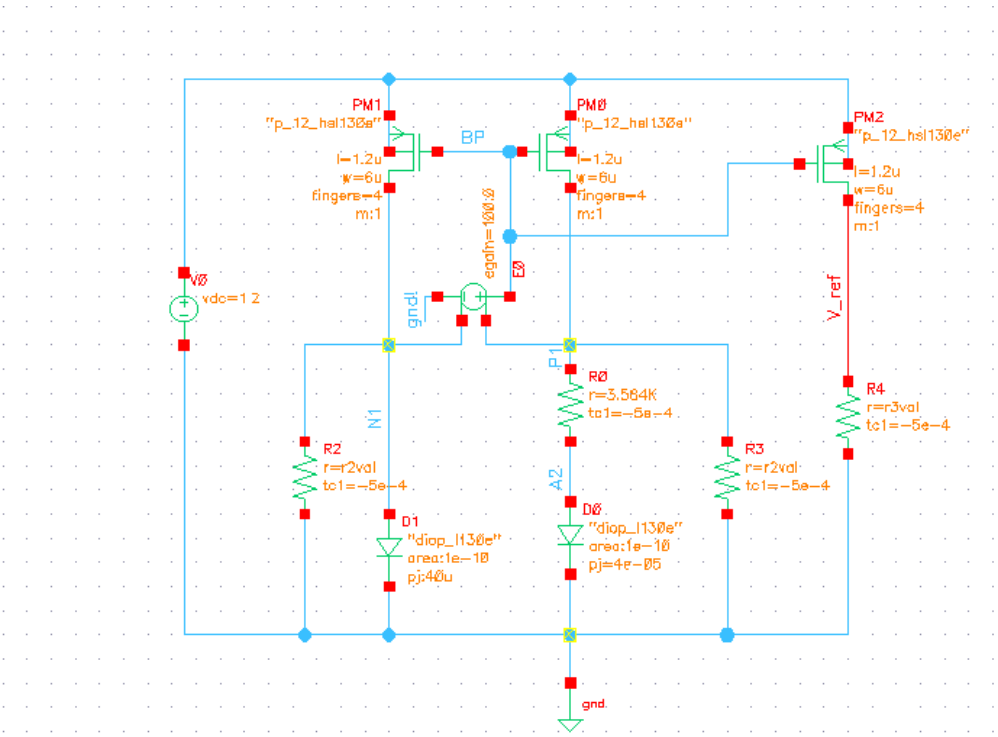


Figure 25: Schematic of the low-voltage band-gap voltage reference entered in Virtuoso SE.

Initial sizing procedure

Following the design equations of the lecture notes (slide 20) and the data for hand calculations (slide 22), the design starts by fixing $I_1 = 10\,\mu\text{A}$ and the multiplicity ratio $M = 4$ (diode D_2 has four times the area of D_1). All thermal-voltage quantities are evaluated at room temperature $T_0 = 300\,\text{K}$, giving $U_T = k_B T_0/q = 25.85\,\text{mV}$.

Step 1 — Resistor R_1 and diode voltage V_{D1}. From the PTAT current equation (1):

$$I_1 = \frac{U_T \ln(M)}{R_1} \implies R_1 = \frac{U_T \ln(M)}{I_1} = \frac{25.85\,\text{mV} \times \ln 4}{10\,\mu\text{A}} = 3.584\,\text{k}\Omega \tag{31}$$

$$V_{D1} = U_T \ln\!\left(\frac{I_1}{I_S}\right) = 25.85\,\text{mV} \times \ln\!\left(\frac{10\,\mu\text{A}}{6.896 \times 10^{-17}\,\text{A}}\right) = 664.4\,\text{mV} \tag{32}$$

Step 2 — Resistor R_2 (zero temperature-coefficient condition). Setting $\partial V_{REF}/\partial T = 0$ at T_0 requires eq. (5):

$$\frac{R_2}{R_1}\ln(M) = \ln\!\left(\frac{I_{S0}}{I_1}\right) \implies R_2 = R_1\,\frac{\ln(I_{S0}/I_1)}{\ln(M)} \tag{33}$$

with $I_{S0} = I_S \exp(qV_{G0}/k_BT_0) = 1.207 \times 10^4\,\mathrm{A}$:

$$R_2 = 3.584\,\mathrm{k\Omega} \times \frac{\ln(1.207 \times 10^9)}{\ln(4)} = 54\,\mathrm{k\Omega} \tag{34}$$

Step 3 — Current I_2. The current flowing through R_2 is set by the voltage across D_1 (eq. 2):

$$I_2 = \frac{V_{D1}}{R_2} = \frac{664.4\,\mathrm{mV}}{54\,\mathrm{k\Omega}} = 12.3\,\mathrm{\mu A} \tag{35}$$

Step 4 — Resistor R_3. Once the zero-TC condition is satisfied, $V_{REF} \cong (R_3/R_2)\,V_{G0}$, so:

$$R_3 = R_2\,\frac{V_{REF}}{V_{G0}} = 54\,\mathrm{k\Omega} \times \frac{0.8\,\mathrm{V}}{1.205\,\mathrm{V}} = 35.9\,\mathrm{k\Omega} \tag{36}$$

Step 5 — Transistor sizing. The gate lengths are set to $L_3 = L_4 = L_5 = 1.2\,\mu\mathrm{m}$ to limit channel-length-modulation errors in the M3–M4–M5 current mirror. Assuming $|V_{OV3}| = 0.3\,\mathrm{V}$ and using the total drain current $I_{D3} = I_{D4} = I_{D5} = I_1 + I_2 = 22.3\,\mathrm{\mu A}$:

$$I_1 + I_2 = \frac{k'_p}{2}\cdot\frac{W}{L}\cdot V_{OV}^2 \implies W = \frac{2\,(I_1+I_2)\,L}{k'_p\,V_{OV}^2} = \frac{2 \times 22.3\,\mu\mathrm{A} \times 1.2\,\mu\mathrm{m}}{100\,\mu\mathrm{A/V^2} \times (0.3\,\mathrm{V})^2} = 6\,\mathrm{\mu m} \tag{37}$$

The same width is used for all three transistors.

Table 13: Component values from the initial sizing.

Component	Parameter	Value
R_1	Resistance	$3.584\,\mathrm{k\Omega}$
R_2	Resistance	$54\,\mathrm{k\Omega}$
R_3	Resistance	$35.9\,\mathrm{k\Omega}$
M3, M4, M5	W	$6\,\mathrm{\mu m}$
M3, M4, M5	L	$1.2\,\mathrm{\mu m}$
M3, M4, M5	#fingers	4

R_2 is instantiated twice (one between N_1 and ground, one between P_1 and ground). All resistors have $\texttt{tc1} = -5 \times 10^{-4}$.

Simulation results — initial design

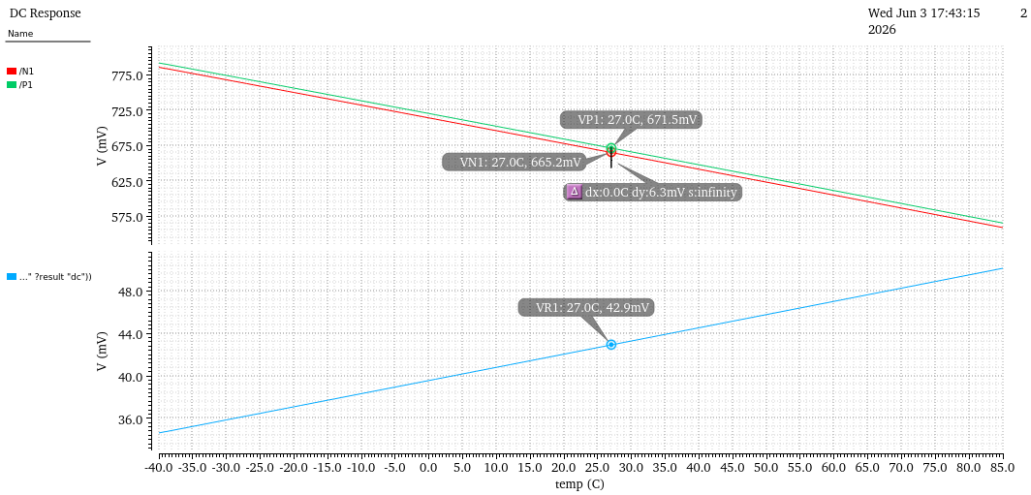


Figure 26: Node voltages vs temperature, initial design. V_{N1} (red) and V_{P1} (green) are CTAT; the blue trace in the lower panel is $V_{R1} = V_{P1} - V_{A2}$, which is PTAT. Markers at $T = 27\,^{\circ}\mathrm{C}$ on V_{N1} and V_{P1}.

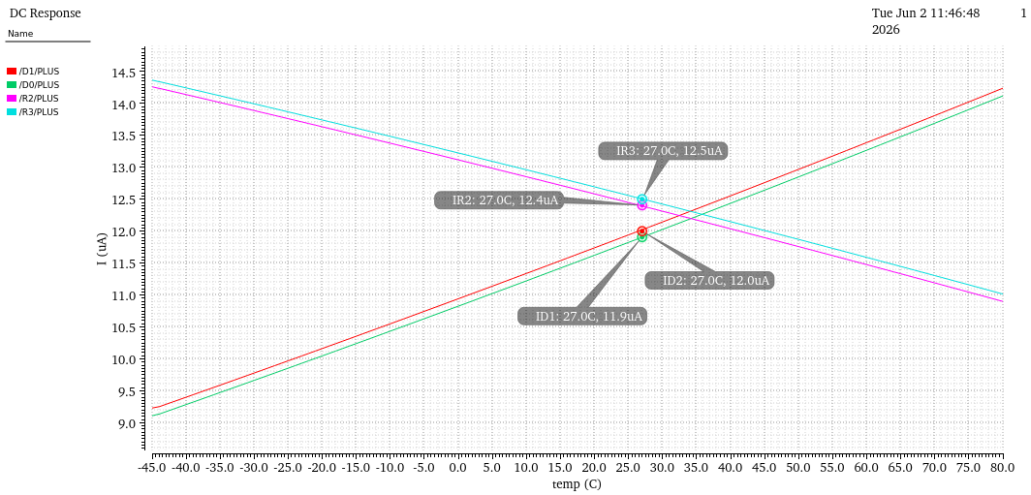


Figure 27: Branch currents vs temperature, initial design. Markers at $T = 27\,^{\circ}\mathrm{C}$.

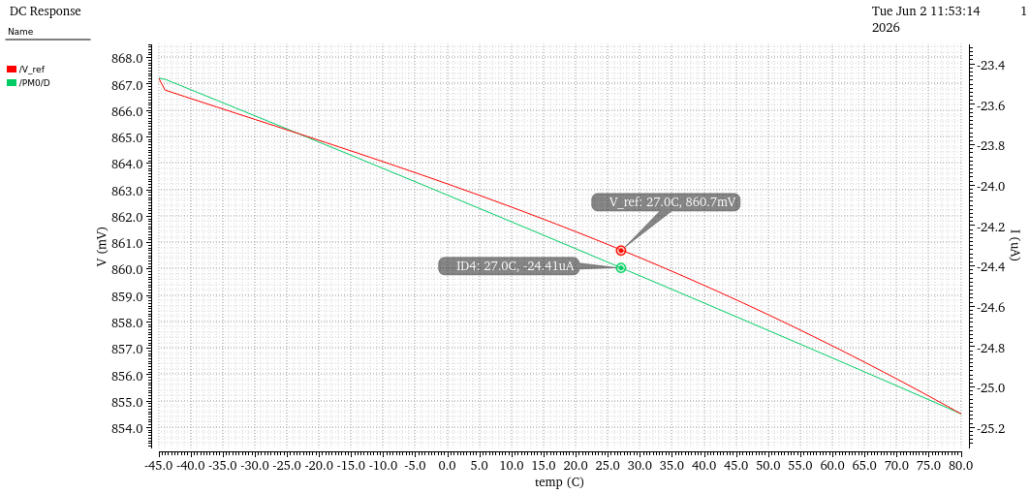


Figure 28: Reference voltage and I_{D4} vs temperature, initial design. Markers at $T = 27\,^{\circ}\mathrm{C}$.

The values at $T = 27\,^{\circ}\mathrm{C}$ and the corresponding fractional temperature coefficients extracted from the three plots of the initial design are summarised in Table 14, together with the expected values predicted by the temperature-dependence model of slide 20. The simulated TC_F values are estimated from the slope of each trace over the full sweep range as $TC_F = \dfrac{1}{X(T_0)}\dfrac{\Delta X}{\Delta T}$.

Quantity	Value @ 27 °C	TC_F sim. [K^{-1}]	TC_F exp. [K^{-1}]
V_{N1}	669.3 mV	-2.5×10^{-3}	-2.85×10^{-3}
V_{P1}	675.2 mV	-2.5×10^{-3}	-2.85×10^{-3}
V_{R1}	43 mV	$+2.9 \times 10^{-3}$	$+1/T = +3.33 \times 10^{-3}$
I_{D1}	11.9 µA	$+3.4 \times 10^{-3}$	$1/T - \mathrm{tc1} = +3.83 \times 10^{-3}$
I_{D2}	12.0 µA	$+3.3 \times 10^{-3}$	$+3.83 \times 10^{-3}$
V_{REF}	860.7 mV	-1.1×10^{-4}	0
I_{D4}	24.41 µA	$+3.9 \times 10^{-4}$	$-\mathrm{tc1} = +5 \times 10^{-4}$

Table 14: Simulated values and fractional temperature coefficients at $T = 27\,^{\circ}\mathrm{C}$, initial design, with expected values from the temperature-dependence model. V_{N1} and V_{P1} are CTAT and differ by the 5.9 mV offset of the VCVS; V_{R1} is PTAT (the offset slightly reduces its TC); $I_{D1} = I_{D2}$ due to the M3–M4 mirror. V_{REF} exceeds the specification of $2 \times 10^{-6}\,\mathrm{K}^{-1}$, motivating the tuning of Sec. 4.2; $I_{D4} = I_1 + I_2$ flows entirely through R_3 at the output.

4.2 Design tuning

The initial sizing ($R_1 = 3.584\,\mathrm{k\Omega}$) yields a reference value of 860.7 mV (about 7.6% above the 0.8 V target) and a fractional temperature coefficient of $-1.1 \times 10^{-4}\,\mathrm{K}^{-1}$, both out of specification. The high V_{REF} follows from the mirror current being larger than nominal: the finite gain of the VCVS introduces a residual input offset of ≈ 6 mV that raises I_1 to $\approx 11.9\,\mu$A instead of $10\,\mu$A. The design is tuned in three steps, following the procedure of slide 25.

1. **Adjust R_1.** Since the simulated $I_1 \approx 11.9\,\mu$A differs from the nominal $10\,\mu$A, R_1 is scaled to $4.2\,\text{k}\Omega$ to bring the PTAT current back close to its design value. V_{REF} drops to 803.1 mV, but the curve is still strongly CTAT ($TC_{V_{REF}} \approx -2.6 \times 10^{-4}\,\text{K}^{-1}$), so the slope must still be nulled.

2. **Adjust R_2.** R_2 is increased to flatten $V_{REF}(T)$ and null the slope at 27 °C. Because R_1 was rescaled, the resistor values are recomputed: with $R_2 = 66.5\,\text{k}\Omega$ and the matching $R_3 = 42\,\text{k}\Omega$, the curve becomes flat at room temperature ($TC_{V_{REF}} \approx 0.87\,\mu\text{K}^{-1}$, with a maximum near 27 °C), meeting the TC specification. The reference, however, overshoots to 843.75 mV.

3. **Adjust R_3.** V_{REF} is brought back to 0.8 V by reducing R_3. Since R_2 and R_3 are coupled through the mirror operating point — lowering R_3 alone degrades the TC — R_2 is also slightly reduced. The final values $R_2 = 65.2\,\text{k}\Omega$, $R_3 = 39.3\,\text{k}\Omega$ give $V_{REF} = 800.687\,\text{mV}$ with $TC_{V_{REF}} \approx 0.66\,\mu\text{K}^{-1}$, both within specification.

A plot of V_{REF} and I_{D4} vs T is taken after each change.

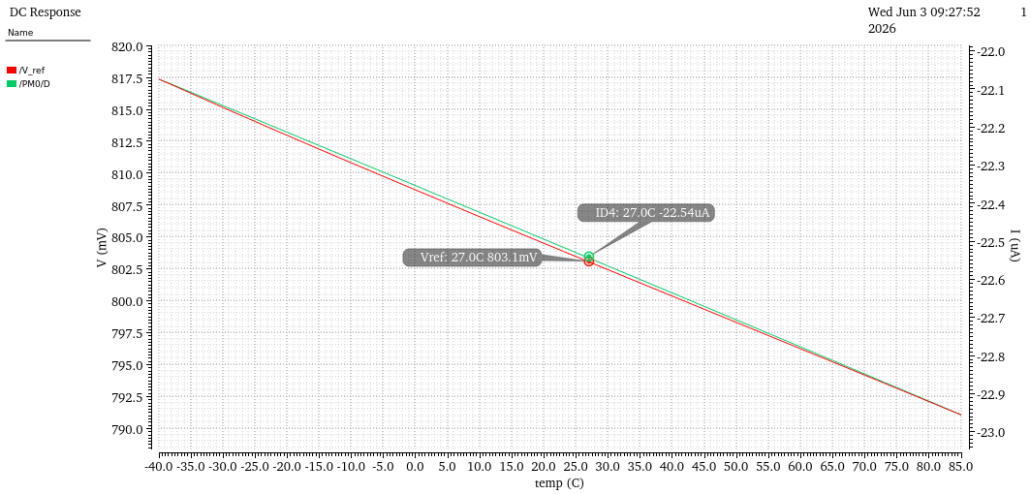


Figure 29: V_{REF} and I_{D4} vs temperature after the R_1 adjustment (step 1, $R_1 = 4.2\,\text{k}\Omega$, $R_2 = 54\,\text{k}\Omega$, $R_3 = 35.9\,\text{k}\Omega$). Scaling R_1 brings V_{REF} close to target (803.1 mV at 27 °C, $I_{D4} = -22.54\,\mu$A), but the curve is still strongly CTAT, so the specification is not met by acting on R_1 alone. Marker at $T = 27\,°\text{C}$.

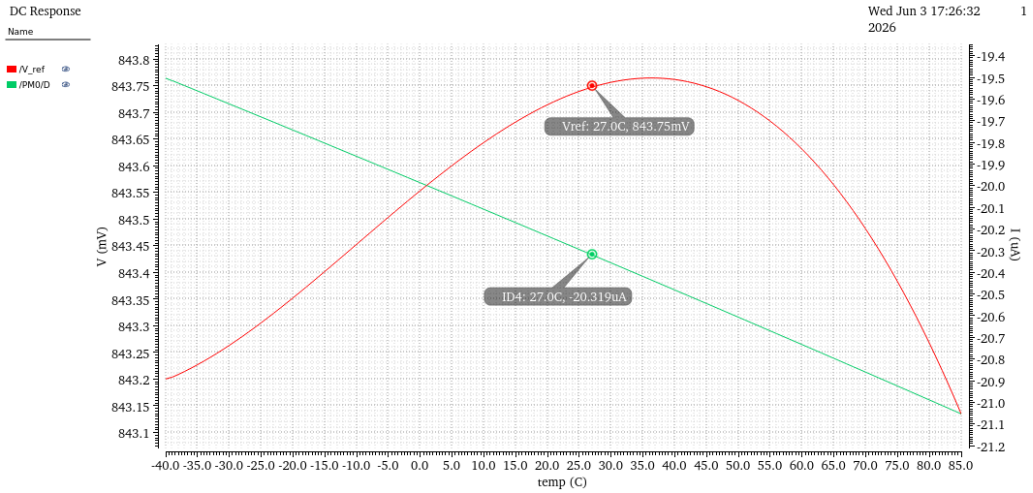


Figure 30: V_{REF} and I_{D4} vs temperature after the R_2 adjustment (step 2, $R_1 = 4.2\,\text{k}\Omega$, $R_2 = 66.5\,\text{k}\Omega$, $R_3 = 42\,\text{k}\Omega$). The slope at 27 °C is nulled ($V_{REF} = 843.75\,\text{mV}$, $I_{D4} = -20.32\,\mu\text{A}$), with a maximum near room temperature, but V_{REF} is above target. Marker at $T = 27\,°\text{C}$.

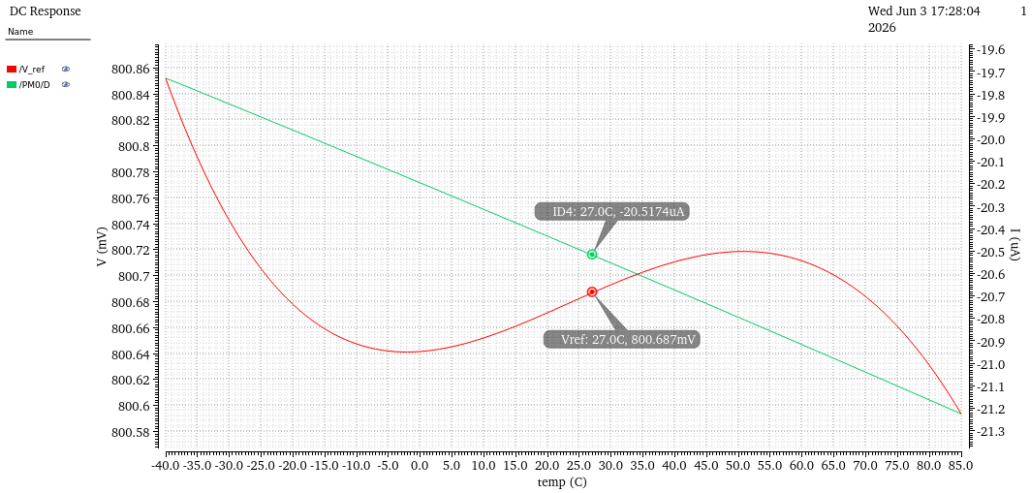


Figure 31: V_{REF} and I_{D4} vs temperature after the final R_3 adjustment (step 3, $R_1 = 4.2\,\text{k}\Omega$, $R_2 = 65.2\,\text{k}\Omega$, $R_3 = 39.3\,\text{k}\Omega$). $V_{REF} = 800.687\,\text{mV}$ at 27 °C, with a near-zero slope. Marker at $T = 27\,°\text{C}$.

Step	R_1 [kΩ]	R_2 [kΩ]	R_3 [kΩ]	V_{REF} @ 27 °C [mV]	$TC_{V_{REF}}$ [K^{-1}]
Initial	3.584	54.0	35.9	860.7	-1.1×10^{-4}
1 (R_1)	4.2	54.0	35.9	803.1	-2.6×10^{-4}
2 (R_2)	4.2	66.5	42.0	843.8	$+8.7 \times 10^{-7}$
3 (R_3)	4.2	65.2	39.3	800.7	$+6.6 \times 10^{-7}$

Table 15: Tuning history: R_1 is scaled to correct I_1 (step 1), R_2 is increased to null the slope (step 2), then R_3 is reduced — with a small R_2 correction — to recentre V_{REF} on 0.8 V while keeping the slope nulled (step 3).

The final design ($R_1 = 4.2\,\mathrm{k\Omega}$, $R_2 = 65.2\,\mathrm{k\Omega}$, $R_3 = 39.3\,\mathrm{k\Omega}$) achieves $V_{REF}\big|_{300\,\mathrm{K}} = 800.687\,\mathrm{mV}$, corresponding to a relative error

$$\varepsilon_{V_{REF}} = \frac{|800.687 - 800|}{800} \times 100\% = 0.086\%, \tag{38}$$

and a fractional temperature coefficient $TC_{V_{REF}} \approx 0.66\,\mu\mathrm{K}^{-1} = 6.6 \times 10^{-7}\,\mathrm{K}^{-1}$. Both figures are within their specifications ($\pm 0.1\%$ on V_{REF} and $2 \times 10^{-6}\,\mathrm{K}^{-1}$ on $TC_{V_{REF}}$). The $V_{REF}(T)$ curve exhibits the characteristic second-order bandgap curvature, with the inflection placed at room temperature.

4.3 Sensitivity of the reference to supply voltage variations

To evaluate the robustness against supply variations, a DC sweep of V_{DD} over 1.0–1.4 V ($\pm 10\%$ around the nominal 1.2 V) is performed, plotting V_{REF} and I_{D4}. The normalised sensitivity of a quantity X is:

$$S^{X}_{V_{DD}} = \frac{V_{DD}}{X_{\mathrm{nom}}} \cdot \frac{\partial X}{\partial V_{DD}} \tag{39}$$

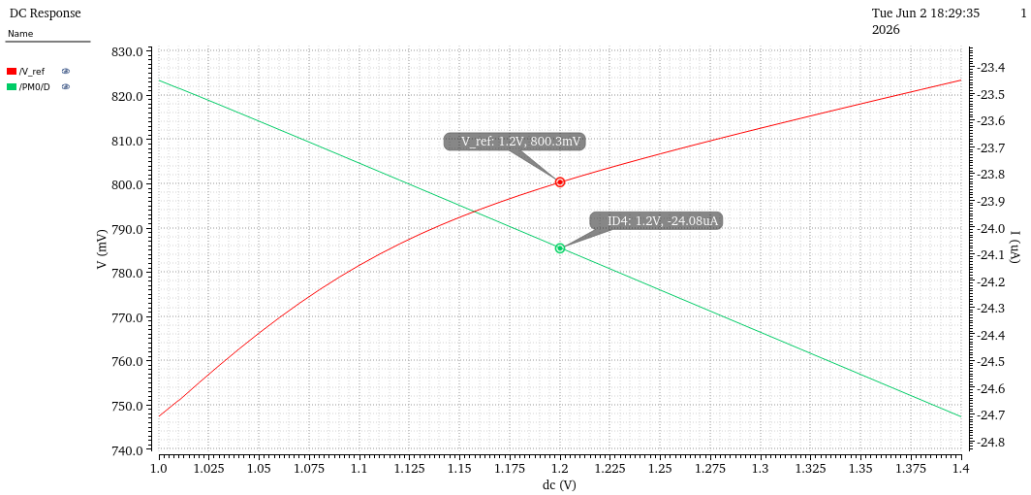


Figure 32: V_{REF} and I_{D4} vs supply voltage. Markers at $V_{DD} = 1.2\,\mathrm{V}$ ($V_{REF} = 800.7\,\mathrm{mV}$, $I_{D4} = -20.52\,\mu\mathrm{A}$).

Estimating the slopes at $V_{DD} = 1.2\,\mathrm{V}$ gives

$$\frac{\partial V_{REF}}{\partial V_{DD}} \approx 0.13\,\mathrm{V/V}, \qquad \frac{\partial I_{D4}}{\partial V_{DD}} \approx 2.8\,\mu\mathrm{A/V},$$

hence

$$S^{V_{REF}}_{V_{DD}} \approx 0.20, \qquad S^{I_{D4}}_{V_{DD}} \approx 0.16.$$

The two values are of the same order, as expected from $V_{REF} = R_3 I_{D4}$ with R_3 supply-independent; the small residual difference is due to channel-length modulation in the M3–M4–M5 mirror, whose finite output resistance limits supply rejection. Cascoding the mirror would improve the figure.